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Optimizing Test System Development: Best Practices Unveiled





Raul Galvez

16-year veteran in the test automation industry specializing in the design, development, and deployment of automated test systems (ATE's) for various types of customers across multiple countries. Certified LabVIEW and TestStand architect as well as a python practitioner with more than a decade mentoring customers and peers ranging from architects to developers. Former employee of Sanmina-SCI (Contract manufacturer), Averna (NI alliance Partner), and currently part of National Instruments (NI) as a Chief Solutions Engineer.





Sergio Velderrain

Mechatronic engineer with 12 years of experience designing solutions using NI software. Former employee of multiple NI partners (Cygnus, Averna, and Konrad). LabVIEW Champion before joining National Instruments and a Certified LabVIEW and TestStand architect. ADAS subject matter expert and founding member of the first ADAS datalogging team for Konrad Germany. Currently part of NI as a Senior Field Applications Engineer for automotive customers in the northern California area.









Adolfo Islas

Electronic Engineer/MBA with 11 Years of Experience as a test system integrator and Reckon Solution commercial manager. Designed and deployed projects for multiple industries ranging from automotive, consumer electronics and telecommunications in Mexico, Canada, USA, Argentina and Brazil. Passionate LabVIEW and TestStand developer currently contributing to the NI community with LabVIEW user groups over social media with over 6.5K users. Content creator and streamer of Developing LabVIEW practices in Twitch and Facebook Live.





AGENDA



- Introduction
- Importance of Test System Optimization
- **Consideration & Best Practices**
 - Project Management
 - Hardware
 - Software
 - **Case Studies**
 - Global validation team
 - **Reckon Lidar ATE**
- Conclusion
- Q&A





Why Test Systems Are Extremely Important?





Test System Depends On Product Phase



DUPLICABLE, RUGGED, AND STREAMLINED







Main Factors At The Time To Plan A Test System









Key Areas When Develop A Test System







Collecting The Test Requirements And Defining The Project Scope Is Really Important!!!.









Total Cost of Ownership(TCO) an ATE (Automated Test System).

+

DEVELOPMENT COSTS

- Planning
- Training
- Tools
- Development Effort
- Development System

DEPLOYMENT COSTS

- Capital Equipment
- Assembly

+

- Software
 Deployment
- Shipping

OPERATIONAL COSTS

- Labor
- Training
- Maintenance
- Spares
- Installation
- Utilities

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TOTAL COST OF OWNERSHIP

- Quantified Financial Impact
- Minimized Test TCO
- Improved Cost/Defect
- Optimized Test
 Organization





Hardware Considerations & Best Practices

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Selecting Instrumentation

"pick the right tool for the job."

Analog Instruments Categories

	DC AND POWER	LOW-SPEED ANALOG	HIGH-SPEED ANALOG	RF A
Input, Measure	Digital Multimeter	Analog Input, Data Acquisition (DAQ)	Oscilloscope, Frequency Counter	RF A (Spec Signa
Output, Generate	Programmable Power Supply	Analog Output	Function/Arbitrary Waveform Generator (FGEN, AWG)	RF S Signa
Input and Output On The Same Device	DC Power Analyzer	Multifunction Data Acquisition (DAQ)	All-in-One Oscilloscope	Vecto
Input and Output On The Same Pin	Source Measure Unit (SMU)	LCR Meter	Impedance Analyzer	Vecto

• Highly recommended to select devices with good longevity in the market, this minimize the risk to have problems for maintenance and get spare parts.

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ND WIRELESS

nalyzer Power Meter ctrum Analyzer, Vector al, Analyzer)

ignal Generator (Vector al Generator, CW Source)

or Signal Transceiver (VST)

or Network Analyzer (VNA)





Selecting Instrumentation

"pick the right tool for the job."

Digital Instruments Categories

	STATIC, LOW SPEED	SYNCHRONOUS AND HIGH- SPEED PARALLEL (100 MBITS/S RANGE)	HIGH-SPEED SE GBITS/S RANGE
Interface (Standard)	Low-Speed Standard Interface (Protocol Interface (ARINC 429,	Card (I2C, C) Synchronous CAN, GPIB, I2C, SPI)	Interface Card (10 Ethernet, Fiber Ch Express, and so o
Interface (Custom)	Digital I/O (GPIO)	Digital Waveform Generator/ Analyzer, Pattern Generator	FPGA-Based High Serial Interface Au Rapid I/O, JESD2
Electrical Test And Timing Test (Basic Interface)	Pin Electronics Digital, Per-Pin ((PPMU)	Parametric Measurement Unit	BERT, Oscillosco

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RIAL (10

) Gigabit hannel, PCI on)

h-Speed urora, Serial 204b/c

ре





Selecting Instrumentation

"pick the right tool for the job."

The Size Matters!

	BANDWIDTH (MBYTES/S)	LATENCY (µS)	RANGE (M) (WITHOUT EXTENDERS)	SETUP AND INSTALLATION
GPIB	1.8 (488.1) 8 (HS488)	30	20	Good
USB	60 (USB 2.0) 640 (USB 3.0)	Analog Output	5	Best
PCI (PXI)	132	0.7	Internal PC Bus	Better
PCI Express & PXI Express	250 (x1) 4,000 (x16)	0.7 (x1) 0.7 (x4)	Internal PC Bus	Better
Ethernet/LAN/LXI	12.5 (Fast) 125 (Gigabit)	1,000 (Fast) 1,000 (Gigabit)	100 m	Good

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CONNECTOR RUGGEDNESS

Best

Good

Better Best (for PXI)

Better Best (for PXI)

Good





Automated Test System Power Infrastructure









Automated Test System Power Infrastructure Power Budget

Equi	oment	Maximum Power Consumption	Average Power Utilization	Current at 110
	Fans	50 W	35 W	0.03 A
	HMI	100 W	70 W	0.06 A
	Ethernet Switch	25 W	17.5 W	0.02 A
PDU1	Overtemp Monitor	10 W	7 W	0.01 A
	PXI System	526.9 W	369 W	3.4 A
	DUT Control Pumps	1,000 W	700 W	6.4 A
PDU 1 Total		-	1,198.5 W	11.0 A
PDU 2	VirtualBench	150 W	105 W	1.0 A
	750 W Power Supply	1,100 W	770 W	7.0 A
PDU 2 Total		-	875 W	8.0 A
System Total		-	2,073.5 W	19.0 A

1. Base your system power requirements on about 60 to 70 percent of the maximum required power of each component

2. Add about 20 percent to the final power calculation from rule one as a safety buffer to account for high-activity periods and any necessary future expansion of the test system.

3. Remember that some items connect through PDUs and UPSs, so there are power subsystems within the larger system.









Automated Test System Power Infrastructure Power Budget

PXIe	-1095					
	PXIe-8880 PXI Controller 123.4 W	PXIe-5162 Oscilloscope 34.8 W	PXIe-4139 SMU 34.65 W	PXIe-6570 Digital Pattern Instrument 68 W	PXIe-4081 DMM 9 W	PXIe-2 Switch M 10 V

$From \rightarrow PXIe-1095 Electrical Specifications$				
Voltage Rail	Maximum Current, Single Power Supply	Maximum Current, Dual Power Supplies		
+5V_AUX	21 W	21 w		
+12 V	900 W	1464 W		
+5 V	107.5 W	107.5 W		
+3.3 V	198 W	198 W		
-12 V	15.6 W	15.6 W		

From→ PXIe-8880 Electrical Specific				
Voltage Rail (V)	Current (Amps) Typical	Current (Amps		
$5 V_{AUX}$	0.95 W	1.15		
+12 V	78 W	104.4		
+5 V	12.2 W	15.55		
+3.3 V	7.4 W	9.8 \		

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tions

- Maximum
- W
- W





Automated Test System Power Infrastructure

Check List	ltem
\checkmark	Power grid voltage standard and configuration
\checkmark	Power grid quality and reliability
\checkmark	Materials compliance like RoHS
\checkmark	Energy compliance like CE, PSE, or KC
\checkmark	Trade compliance and import/export regulations

System Design Factory Deployment

System Design

Factory Deployment









Automated Test System Power Infrastructure Best Practices For Components

Consider younger devices on the market where the EOL is not nearby.

Sourcing commercially available components from an established vendor is a longer-term strategy rather than creating custom parts.



Working closely with a vendor would allow you to identify direct replacements for EOL devices, as well as new products on the pipeline.

It is a best practice to consider standard components rather than creating custom parts.

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Design and plan your system for future expansion.





Rack Layout and Thermal Profiling

System Layout Instrument Blocking Airflow

System Layout Instrument Proper Airflow













Switching and Multiplexing

No Switching





Switching In Test Rack Only



Switching In Test Rack & Fixture







Switching and Multiplexing

				Below 🔵 Average
	FLEXIBILITY	THROUGHPUT	СОЅТ	LOW-LEVEL MEASUREMENTS
No Switching	0		0	
Switching in Test Rack		\bigcirc		0
Switching in Test Fixture	0	\bigcirc	\bigcirc	\bigcirc
Switching in Test Rack and Fixture		\bigcirc	\bigcirc	\bigcirc

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Switching and Multiplexing

Selecting The Right Relay Option For Our Test Solution Is Crucial"

Below O Average O

CAPABILITY	Electromechanical Relay (EMR)	Reed Relay	Field-Effect Transistor (FET)	Solid State Relay(SSR)
High Power		\bigcirc	0	\bigcirc
High Speed	0	\bigcirc		\bigcirc
Small Package Size	\bigcirc			
Low Path Resistance		\bigcirc	0	\bigcirc
Low Voltage Offset	\bigcirc	0	\bigcirc	
Extended Lifetime	0	\bigcirc		











Mass Interconnect and Fixturing









Mass Interconnect and Fixturing







- A. ITA Enclosure
- B. ITA Patchcords
- C. ITA Modules
- D. 9025 ITA

- E. Receiver Cable Assembly
- F. 9025 Receiver
- G. Receiver PCB Adapter
- H. Receiver Module

- I. Receiver Patchcords
- J. Mounting Flanges
- K. Instrument Bracket
- L. Slide Kit





Hardware Considerations To Build a Fixture

		Below 🔘	Average
ABSTRACTION OPTION	CABLES	MASS INTERCONNECT WITH CABLES	MASS IN PCBS (
Frequent Changeover Between DUTs	0		
Optimized For Design And Characterization		0	
Optimized For Verification And Validation (V&V)	\bigcirc	\bigcirc	
Optimized For Test Production	0		
Signal Quality	\bigcirc	\bigcirc	
Continuity of Performance (system to system)	\bigcirc	\frown	
Ease of System Maintenance And Upgradability	0		
System Reconfiguration (that is, scalability)	0		
Ease of Duplication (for example, global deployments)	0	\bigcirc	
Instrument To Module Pin Efficiency	0		
Repairability In The Field			
Instrument Card Rev. Control Tolerance			







System Maintenance

DESIGN GUIDELINES	PREDICTIVE	PREVENTIVE	COF
Self-Test and Monitoring	Condition monitoringVerifying functionality	Verifying functionality	 Detecting failur Diagnosing and Verifying function
Modular Design	 Condition monitoring Servicing Replacing Calibrating Verifying functionality 	 Servicing Replacing Calibrating Verifying functionality 	 Detecting failur Diagnosing and Repairing Verifying function
Standardization	 Condition monitoring Servicing Replacing Calibrating Verifying functionality Improving consistency of work 	 Servicing Replacing Calibrating Verifying functionality Improving consistency of work 	 Detecting failur Diagnosing and Repairing Verifying function Improving construction
Simplicity	 Lowering documentation and training costs Improving consistency of work 	 Lowering documentation and training costs Improving consistency of work 	 Lowering docut costs Improving const
Environment and Human Factors	 Lowering frequency of predictive maintenance events Reducing human errors Improving safety 	 Lowering frequency of preventive maintenance events Reducing human errors Improving safety 	 Lowering failure Reducing huma Improving safe

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Case Study 1: Global validation lab

- Multiple validation labs within a global semiconductor company are using their workbenches to automate their manual validation.
- This company recently switched from a DIY solution that each validation lab implemented, normally by a single person that took the initiative, to the use of TestStand as a company-enforced test executive.
- Now, all validation labs have a centralized location where all sequences can be accessed, which are maintained by a team of 200+ validation engineers spread across multiple facilities.
- This new approach of using TestStand as a standard for automation has greatly increased profitability due to the number of devices under test that can be passed through the test sequence, allowing management to schedule more projects due to the increased bandwidth.
- As time goes by... product increases in complexity. Management is now having to push back again on validating new silicon due to issues on replicating validation results across multiple labs, as well as not being able to validate parts fast enough.

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Case Study 1: Global validation lab



1.- Coupling and technical debt

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- - 4.- No strategy when using source code control

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5.- Not making use of commercially available deployment tools

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6.- Not having a standardized error handling strategy

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Coupling and technical debt

- An automation expert has been brought into the company. Upper management then gave him full control on defining a company-wide approach for automation across all sites.
- After careful evaluation, an initiative was created that would roll out on 2 stages.

STAGE 1	 Challenging the status quo. "This is how we have always done phrase. Identifying areas to define trainings and a mentoring progrengineers ramp up on TestStand. Have the multiple managers from the multiple validation labs understand individual needs that each site has.
	 A mechanism to automate enforcing best practices is embedd code control. Now, if a developer does not adhere to a rule, it is automatical
STAGE 2	 All reuse code is then modified to adhere to these best practice
	established workflow using source code control.

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ram to help validation

align on this plan and

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ally rejected by

es, following an

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Result collection strategy

- NI SystemLink enterprise was chosen for result collection due to the company wide access to results that this product would bring.
- Enabling this result processing plugin on TestStand would automatically post results to the network, no changes to sequences are necessary if the sequence is designed to use a results processing plugin.

Re	esult Processing							
ctive	e Configuration:	<default for<="" th=""><th>Inline Pro</th><th>cessing></th><th>•</th><th>Reset to Defaults</th><th>Advanced</th><th>I</th></default>	Inline Pro	cessing>	•	Reset to Defaults	Advanced	I
	Output Name	Enabled	Display	Options		New Thread		\wedge
\$	Report			ATML 5.00 Standards Report Document (tr5_horizontal:	28	Yes	v	
	Database			Generic Recordset (NI)	2	Yes	~	1
1	Offline Results File			C:\Users\Public\Documents\National Instruments\Test:	38	Yes	~	1
_								٧
ł	Help Show	w More Optio	ns			QK		Cano



Device utilization and calibration forecasting





Asset tracking

🗱 👻 Asset Manager										
Asset Manager > Assets										
Dashboard	1	Export	t all to CSV Compare Ava	ailability Delete Stat	us 🔻				93 of 93 assets	Filter
Assets			System †	Name	Serial Number	Model	Vendor	Firmware Version	VISA Resource Name	Slot Number
Calibrated Assats		Con	nected (43)							
Galibiated Assets		٥	88803Demo1	Dev1	01802E9A	NI USB-60090EM2	National Instruments	1		
Reports		٥	88803Demo1	GPIB0	030CDEF2	NI PCI-GPIB	National Instruments	ì		1
		٢	88803Demo1	88803Demo1	030D0A62	NI PXIe-8880	National Instruments	2.0.1f0		1
		٥	88803Demo1	PXIChassis1	V08X192E1	NI PXIe-1082	National Instruments	: 1.0.0f0	PXI0::1::BACKPLANE	
		٥	88803Demo1	FGEN	00EA9BCF	NI PXIe-5442	National Instruments	1	PXI18::0::INSTR	2
		٥	88803Demo1	HSDIO	00F3053A	NI PXIe-6548	National Instruments	5	PXI23::0::INSTR	4
		۵	88803Demo1	SCOPE	00F4B857	NI PXIe-5122	National Instruments	1	PXI21::0::INSTR	3
		٥	88803Demo1	DCPOWER	0190FF3D	NI PXIe-4143	National Instruments	1	PXI9::0::INSTR	5
		٥	88803Demo1	DMM	00DFDADB	NI PXI-4071	National Instruments	1	PXI15::14::INSTR	6
		ø	88803Demo1	SWITCH	00F45BC1	NI PXIe-2532	National Instruments	1	PXI13::0::INSTR	8
		٢	DESKTOP-9SJHA00	Desktop1	01DF93F4	NI cDAQ-9184	National Instruments	1		
		ø	DESKTOP-9SJHA00	DESKTOP-9SJHA00	516VCV2	Precision 3630 Tower	Dell Inc.	1.1.6		
		٥	DESKTOP-9SJHA00	GPIB0	01C09BB4	NI GPIB-USB-HS	National Instruments	1		
		٥	DESKTOP-9SJHA00	Fluke45	5005161	45	FLUKE	1.6 D1.0	GPIB0::8::INSTR	
		٥	DESKTOP-HUC9K9P	DESKTOP-HUC9K9P	518TCV2	Precision 3630 Tower	Dell Inc.	1.1.6		
		ø	DESKTOP-HUC9K9P	Virtual Thermal Asset 1	12345	Virtual Thermal Asset	Acme	1.0A		
		٥	DESKTOP-HUC9K9P	Fixture 1234	01BB877B	Battery Test Fixture	Acme			1
		٥	NI-cRIO-9042-01E10AB4	RIO0	01E10AB4	cRIO-9042	National Instruments	1		
		٥	NI-cRIO-9042-01E10AB4	cRI01	01E10AB4	NI cRIO-9042	National Instruments	1		
		٥	NI-cRIO-9042-01E10AB4	Mod1	01E0FF7D	NI 9210	National Instruments	1		1
		٥	NI-cRIO-9042-01E10AB4	Mod2	01DF3ABC	NI 9482	National Instruments	1		2
		٥	NI-cRIO-9042-01E10AB8	cRI01	01E10AB8	NI cRIO-9042	National Instruments	1		
		٥	NI-cRIO-9042-01E10AB8	RIOO	01E10AB8	cRIO-9042	National Instruments			
		٥	NI-cRIO-9042-01E10AB8	Mod1	01E0FF76	NI 9210	National Instruments	1		1





Accessibility to results

*	 Test Monitor 													
=	Test Monitor > Test Results	5												
•	Dashboard	Ú,	Downie	oad Attachm	ients	Delete	View TD	MS Data	Export To CSV 👻		Save Query	7 of 7 to	est results	Filter displayed test results
	Motherboard Tests	Gi	roup by	n [Non	e		•						
	NI-9218 Dashboard	Q	uery by	r.	+	Property		-						
	Rocking Fords				×	Status		Ŧ	equals 👻	Pa	assed	*		
	Failure Pareto				×	Started Wit	thin	•	2	\$	Day(s)	*]	
•	Products			Product			Test Program	n	Secial Number	*	System	El	apsed Time	Started At 🍦
	Batteries		ø				Computer Mo	otherboard T	12345		USAUSLT-0944153	3 10	.80 s	October 18,
			ø	154119E-	01L-(01	Manufacturin	ng Test.seq	204268		ATE 2	9.3	79 s	October 18,
	C Series		ø	154119E-	01L-(01	Manufacturin	ng Test.seq	763963		Desktop 2	3.	11 s	October 18,
•	Test Results		٥	154119E-	01L-(01	Manufacturin	ng Test.seq	518866		Desktop 1	3.	37 s	October 18,
	slups		٥				Power Test.s	eq	868404		Desktop 2	1.1	39 s	October 16,
	Falled FVI		ø				Computer Mo	otherboard T	370483		Desktop 1	5.0	06 s	October 16,
	NI-9218 Results		ø				Computer Mo	otherboard T	677990		Desktop 1	5.0	05 s	October 16,
	Test Cell													
•	Reports													
	Failure Pareto													
	NI-9218 Failures													





Network independent result collection

"Test Monitor Client" has a service called "Store and forward".



COAACT



No more "babysitting" parts...

- Very busy product experts were unable to delegate running multiple parts to technicians, due to the room for mistake when typing in a part number or selecting the wrong sequence.
- A modified version of the TestStand sequential process model was created that automated reading the part number via JTAG. No more manual typing.
- Additionally, a new feature was added that sent the status of the test to a mobile device. This way the very busy product expert is able to track multiple technicians running parts on multiple benches across multiple labs.



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Employ Abstraction Layers to Mitigate Risk



COAAGT



Hardware Abstraction Layer (HAL)

- Identify common functionality.
- What are the functions of a DMM?
- What are the functions of a power supply?







Measurement Abstraction Layer (MAL)



connect

NI DMM & NI Switch driverspecific calls



How do the HAL / MAL fit together?





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Source code control(SCC)



- Code traceability
- Long term efficiency increase
- Simplifies collaboration and workload distribution



Git hooks and unit testing

- Unit testing is a tool for automating testing your source code against a specific condition.
- Unit testing was added to source code control. If your code fails the unit test, you can't commit until you pass it.
- In this case, **ONE** simple unit test made collaboration seamless: **IS THERE A BROKEN ARROW?**
- More tests were added later, that enforced good practices by adding VI Analyzer test with specific good practices that want to be enforced on the source code.
- This approach comes with its risks:
 - Too much unit testing would make committing a new feature very restrictive, adding overhead. —
 - **Not enough unit testing** would give the false impression that you didn't broke any rules. -

But, when properly defined, this allows for architects to enforce project rules without having to make code review for each of the commits.

Bad code that gets committed... stays bad. - Chris Roebuck





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Deployment





Package

Installer



Deployment

🔹 👻 Systems M	lanager				
Systems Dashboard 🔉	Managed Systems > NI-cRIO-9042-01E10AB4 >	> Software			
Available	Category - Maintainer - View -	- Clear	Filter		
Installed	Name	Maintainer	Installed Version		
installed	CompactRIO Support	National Instruments	19.0		
Feeds 🖑	HTTP Client with SSL Support	National Instruments	19.0.0		
	LabVIEW Real-Time	National Instruments	19.0		
	NI Scan Engine	National Instruments	8.0.0.49152-0+f0		
	NI System Configuration	National Instruments	19.0		
	NI System Configuration Remote Support	National Instruments	19.0		
	NI opkg arch generation script (python3)	National Instruments	1.0		
	NI-DAQmx	National Instruments	19.0		
	NI-RIO	National Instruments	19.0		
	NI-RIO IO Scan	National Instruments	19.0		
	NI-RIO Server	National Instruments	19.0		
	NI-TimeSync Time Reference for IEEE 802.1AS-	National Instruments	19.0		





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4.- No strategy when using source code control

Source code is used as a "file share" only, there is no way of knowing if a remote has a working copy.

5.- Not making use of commercially available deployment tools

It is known that setting up a workstation can only be made by the validation engineer who has learned the most about NI Software, which are no more than a couple per site.



6.- Not having a standardized error handling strategy

Test sequences are constantly stopping the test due to mistakes that were made by the developer.

CONACT



Error handling strategy

- Things happen such as error codes, timeouts, infinite loops. There is no utopia and it i should be expected that errors will occur.
- In this case, we needed assurances that if an error occurs, there would be a mechanism to protect critical components of the system.
- By making use of the already existing deployment infrastructure made on previous stage of this project, we were able to deploy TestStand files that are components of the custom sequential process model.
- This validation lab no longer has validation boards that are one of a kind, soaked in water due to an instrument that injects cold air being left on since it had the misfortune of an error happening in the middle of injecting cold air.



Which framework is the best?

Actor Framework













Lidar PCBA Test system

Challenge : 1 .- Multiple Board Testing + 2.- Different Final Customer Customization





Mass Interconnection Harness (Sectoring signal model)



Fixture Wireless PCBA interface - Mirror signal contacts







Development Environment



NI LabVIEW **Object Oriented Programming**

MainSequence		- *	Sequences	
Swp	Description	Settings	Sequence	Core
i Sehap (1)			ProcessSetup	Tex
Propety Loader	Property Loader		ANUT	
(End Group)			ManSequence	
Main (25)			PostUUT	
Lost GND	Call Lost GND in (Current File)		ProcessOcanup	Test
			Cuana Volageo	
Power Up	Call Power Up in cCurrent Fileo		Edenal Vatage During Shatdown	
			Control Voltages	
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			Chuler Village	
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	(1)		Enverted Voltage	
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and the second s	the second roughts contact they			
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Discharge	Call Discharge in «Current File»			
(End Group)			c	
General D			Secondary Vacidity	





Run-Time Environment











