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2024 AUSTIN

Implementing Dynamic Wide-Bandgap Device Reliability Testing

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The big change!

Our world is power electronics

- Green energy is linked to electrical power
- E-Mobility is the definition of “power electronic” today
- Power electronic is a luxury good when we think of transportation, elevators, heat pumps or air conditioning

Global energy hunger drives entire industry to limits

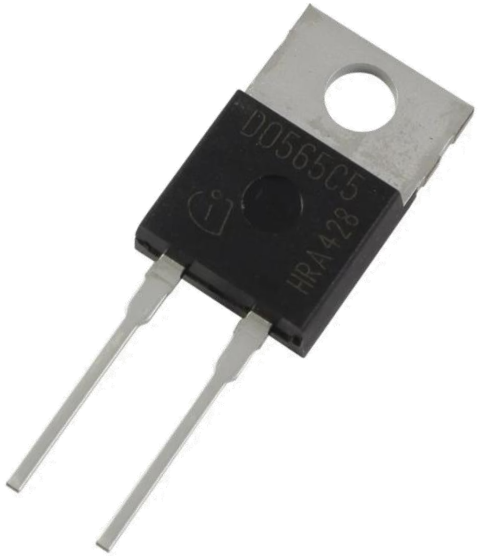
Where Si based transistors and IGBTs did a great job the last 40 years today’s applications e.g. Heat pumps, PV (photo voltaic), EV (electrical vehicle) and even electric air vehicles like EVTOLs (electric vertical take of and landing) or local and decentralized smart grid networks require

- Higher voltage bands
- Higher current ratings
- Better thermal behaviour
- Less power losses
- Faster switching
- Reduced size and wight

higher efficiency

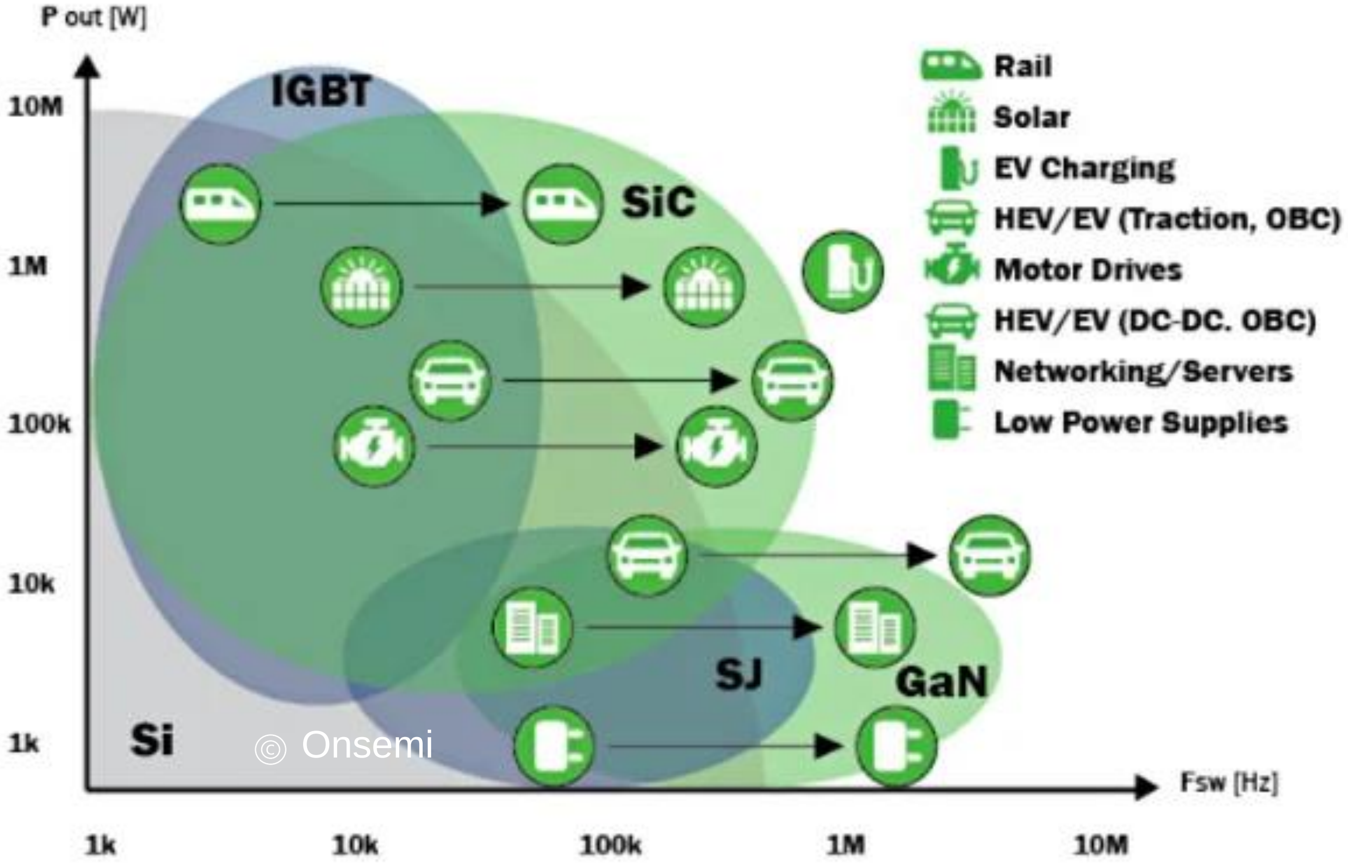
The answer is easy & old: We move to WBG materials !

- In the mid 1970s SiC was under research for use as a new WBG material and late 1980s successfully applied under lab conditions
- Took another 20 years to release the first product to the market
  - in 2001 the first SiC Schottky diode by Infineon !!



Power Semiconductor market: Silicon vs. Wide-Bandgap

- Another 20years in the future the wide application of WBG devices is reality!
- We see a **massive shift from silicon to WBG** materials in high performance applications
- New technologies on old substrate like Super Junction MOSFETs bride the gap
- The **EV (electric vehicle) industry is THE main driver** for WBG power semiconductors, for both SiC and GaN



SI & GaN Reliability vs Silicon Reliability

Reliability Tests Si vs. SiC

- There are decades of investigation and in-field experience available for Si, together with deep understanding of failure modes, acceleration factors, and probabilities

- Based on that knowledge the qualification for Si could be optimized:
  - Tests with high acceleration factors
  - Tests only needed with small engineering samples
  - Tests not needed anymore

- The Situation is **fundamentally different for SiC or GaN**!

Reliability Tests Si vs. SiC

- For SiC/GaN, we need to restart the whole process of selecting and optimizing qualification tests – we can not simply adapt Si reliability testing without verifying first.

- SiC/GaN technologies need
  - a deeper understanding of failure modes
  - data on acceleration factors
  - insight into new effects that have application impact caused by the WBG characteristics

Disruptive EV WBG market!

Time to market is king,

Power Semiconductor devices built into cars are not available in series form years in advance – EV runs on newest gen.

The challenge is to test ~20years of car live within ~1year!
Or 30y green energy solar / wind inverter within ~1 year
… or train inverter, washing machine, etc etc

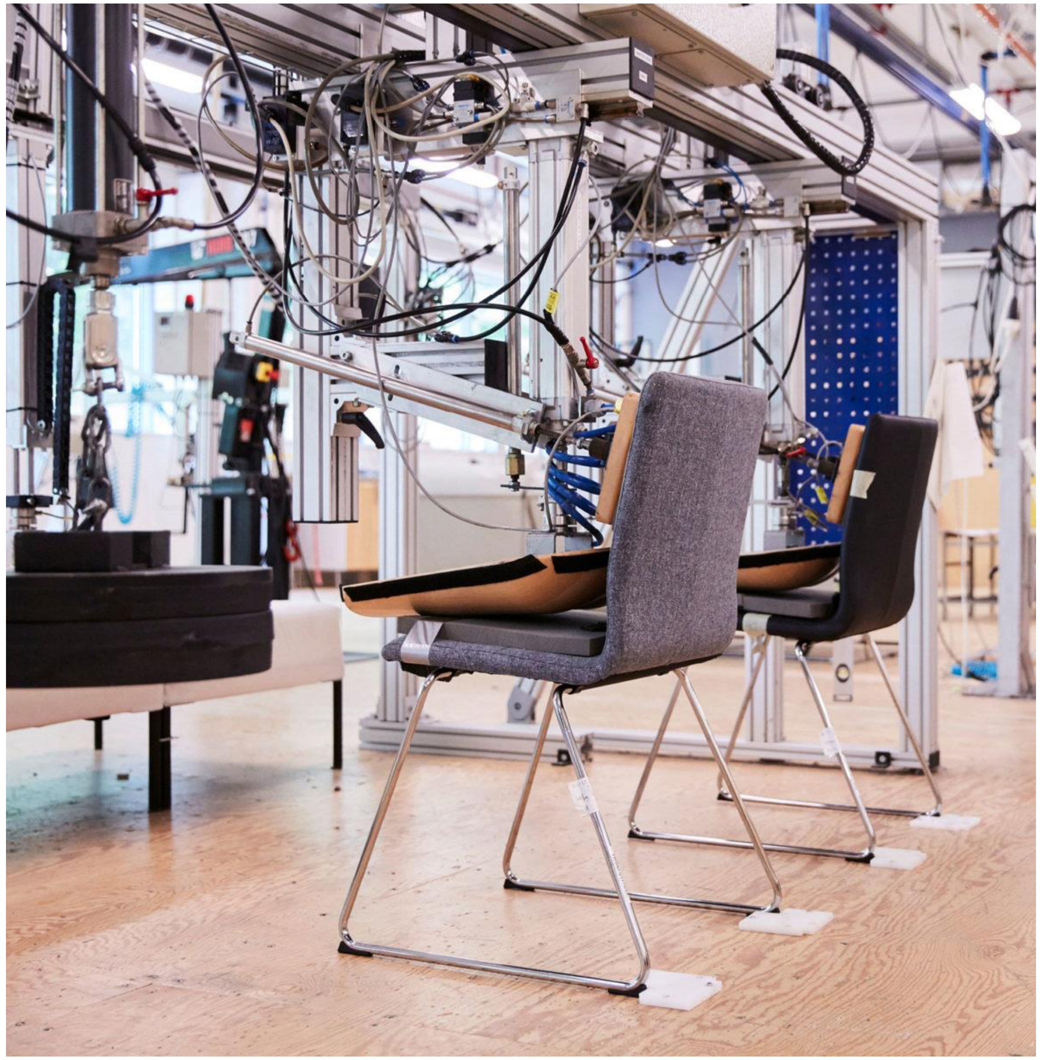
Test 20years within 1 year

We need to accelerate the testing –
preferably 20 years within 1000h!

… that is an acceleration factor of
x175 for components that are always on

Can that be done for chairs?

In picture we have highly accelerated
“chair sit down”



chair testing at IKEA

Today – lets dive in!

In this presentation we'll dive into 2 of failure modes:

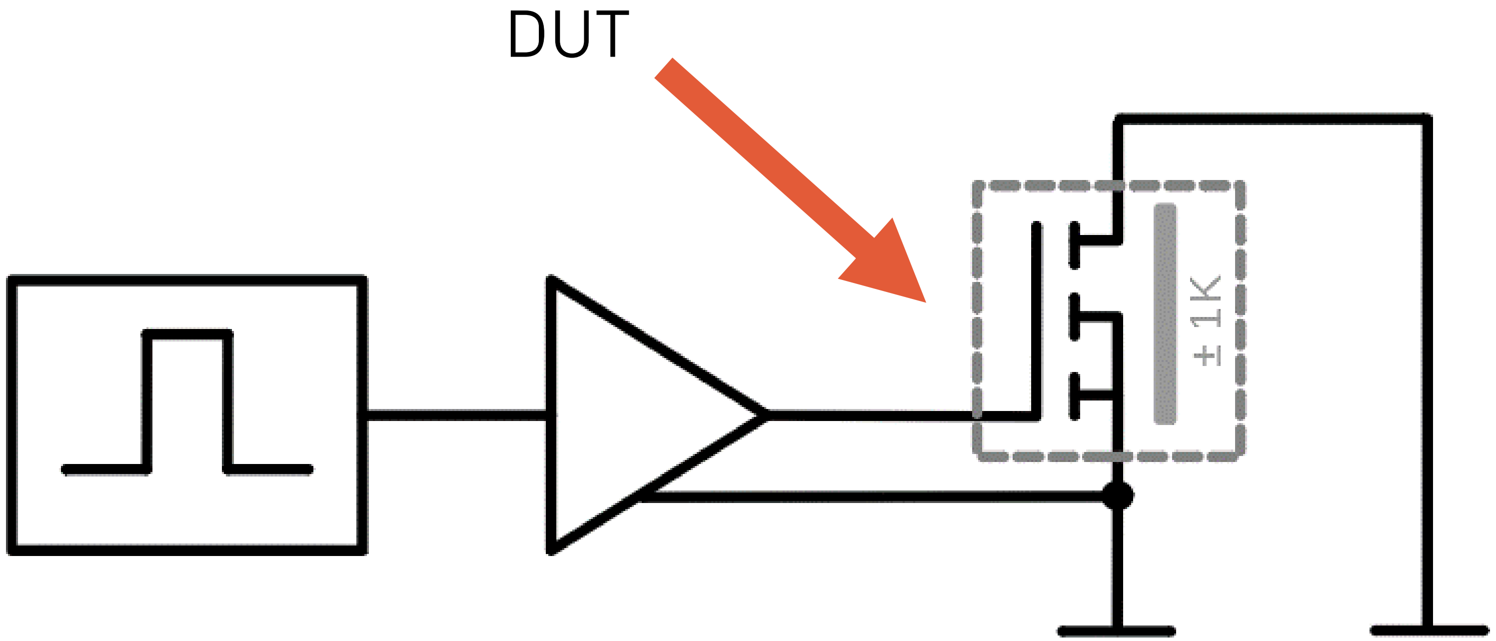
~~People taking a seat~~ => Gate Switchings => DGS/DSS
~~Fabric UV light exposure~~ => Switching in Humidity => dyn H3TRB

Implementing DGS/GSS

DGS / GSS

- Stimulating the gate of a DUT with high d*V*/d*t* edges

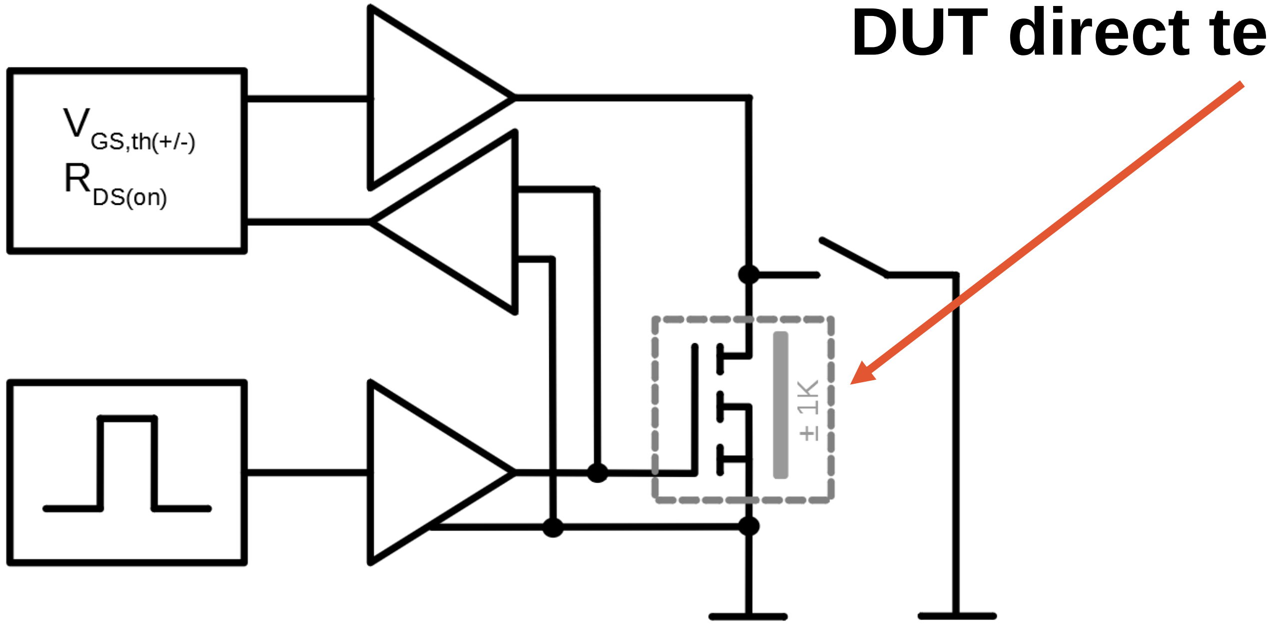
150 kHz to 500 kHz
~0.1 to 1 V/ns d*V*/d*t*
$V_{GS,min/max}$ Datasheet


DUT

DGS / GSS

- Stimulating the gate of a DUT with high dV/dt edges
- Measurement of threshold voltage and $R_{DS,on}$

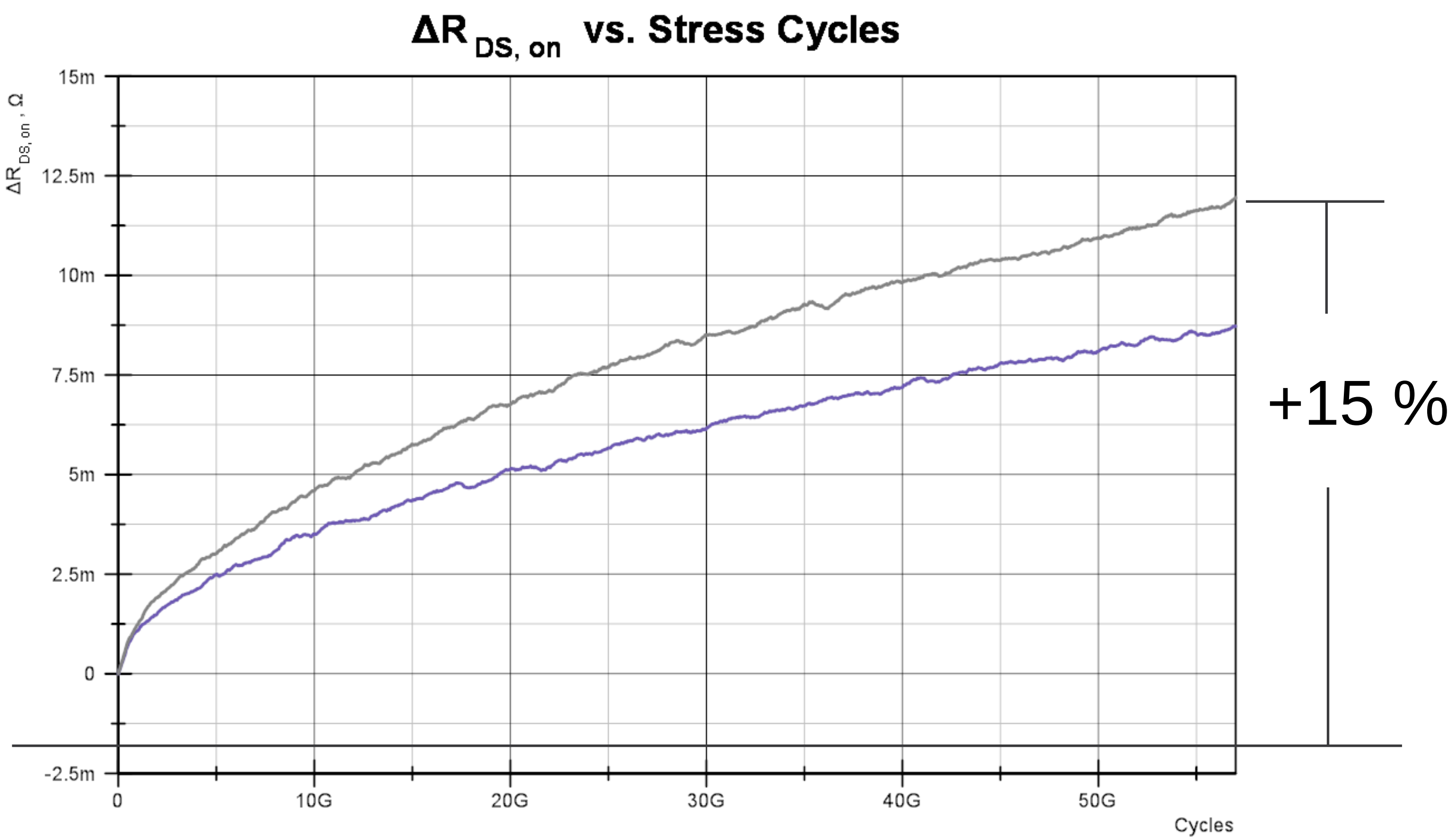
100 ms Pre-Conditioning
$V_{GS,th}$ @ 10 mA
$V_{GS,th\pm}$ (up/down)



DUT direct temp controlled

Why does it matter?

- effect happens in application, with FET usage within datasheet values
- It does not necessarily lead to a shorter lifetime but to reduced performance over lifetime.
- Our measurements show no path to create dynamic HTGB impact model from static HTGB test results



+15 %

≈ 1/10th of car life

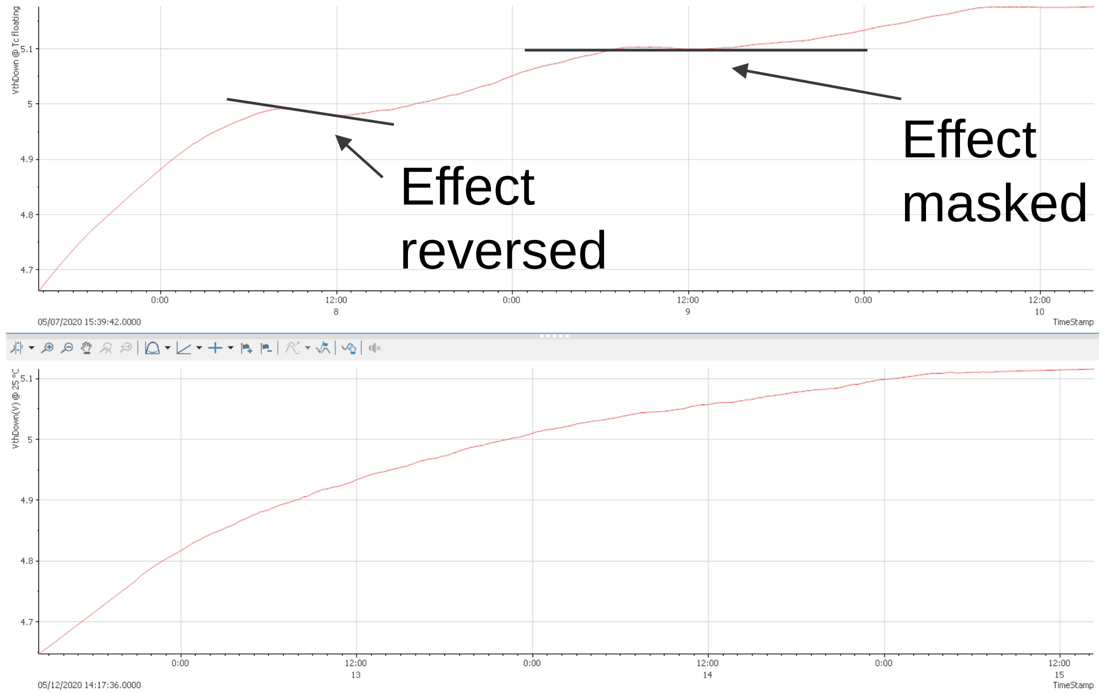
DGS/GSS

To make sure all effects could be identified, a test system with in-situ capabilities was used

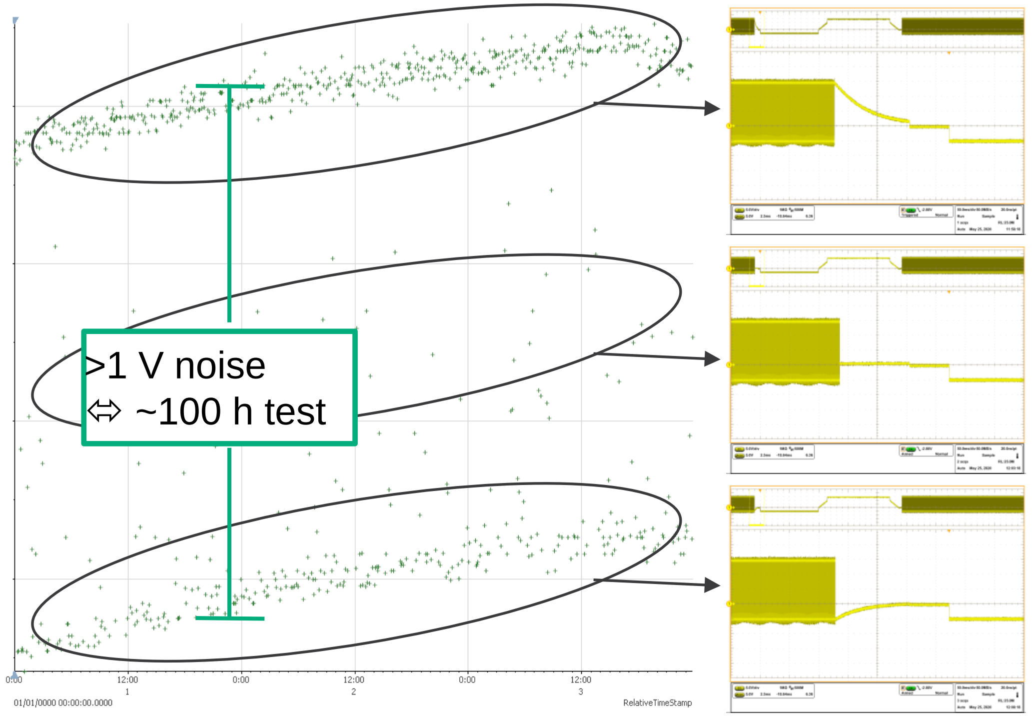
- Free configurable measurement cycles
- Stable and configurable Δt between test and measurement

DGS/GSS

The high number of measurements helped to identify $V_{GS,th\pm}$ measurement challenges that are not easily visible in normal setups.

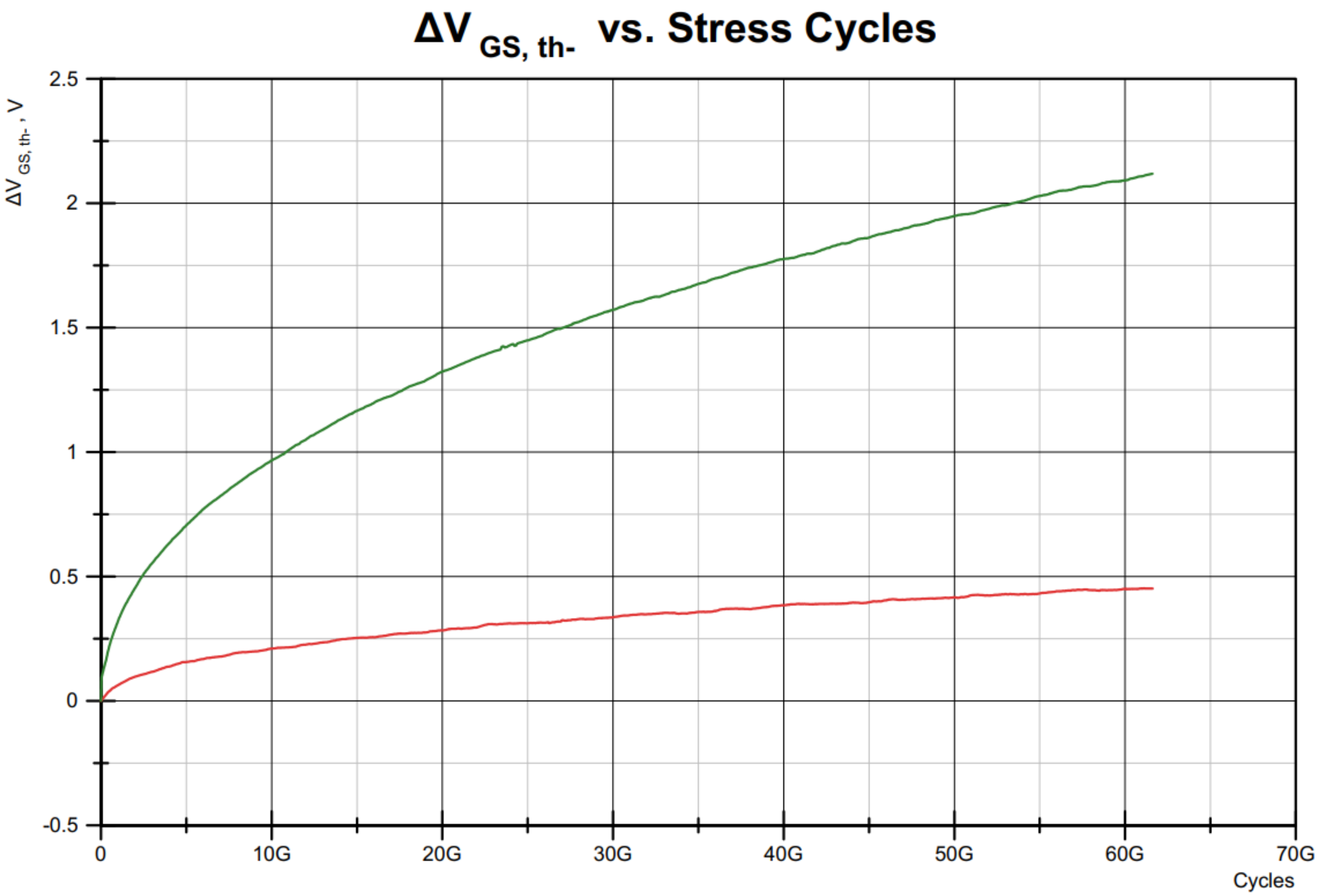


Effect masked or reversed by not considering temperature



Measurement noise due to insufficient preconditioning after stimuli – Noise error higher than 100 h drift effect

Voltage Dependency



V_{GS}: -4 V/18 V (red)

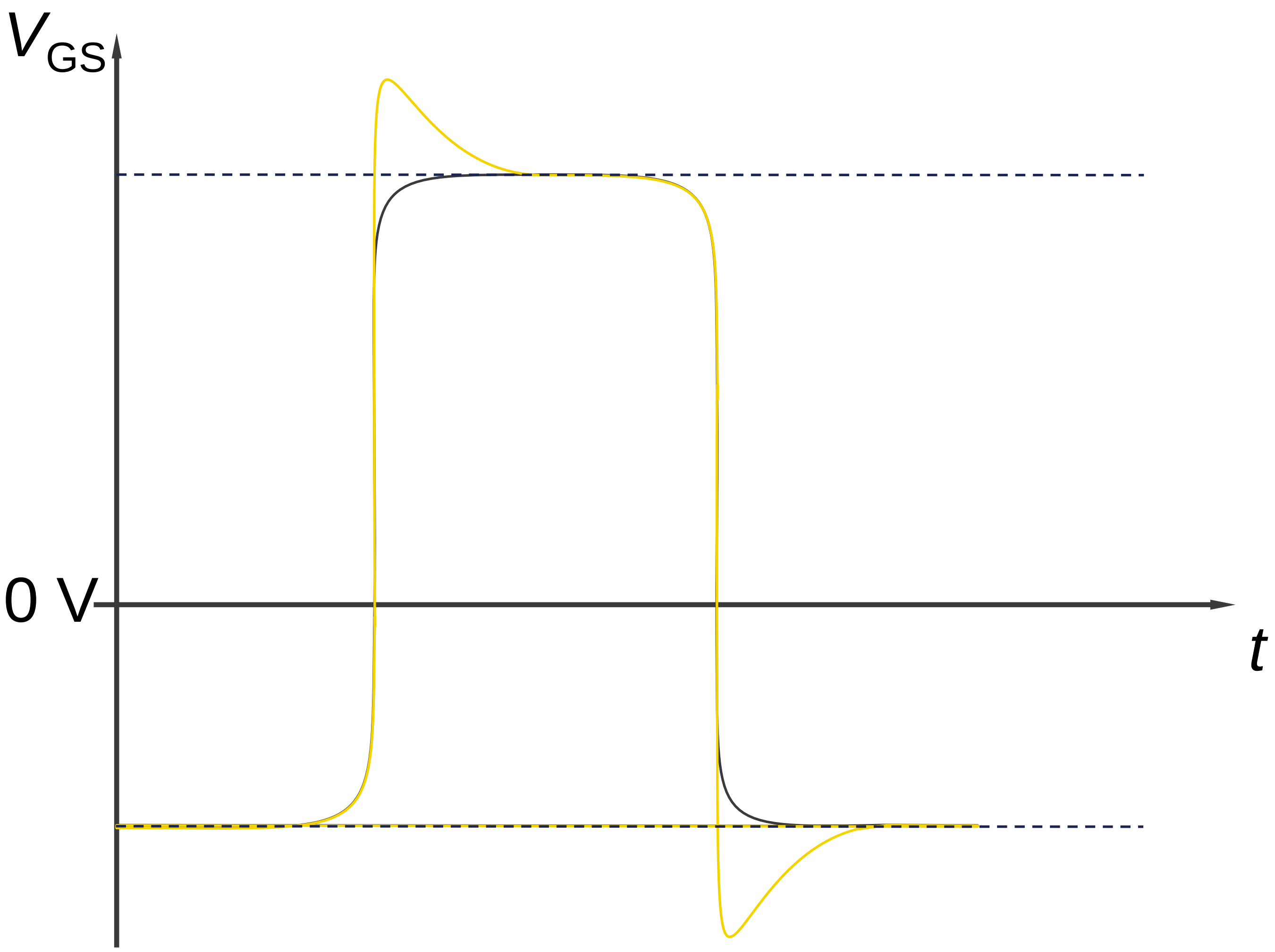
-8 V/18 V (green)

f: 100 kHz

T_c: 25 °C

Voltage Dependency

- Voltage Overshoot



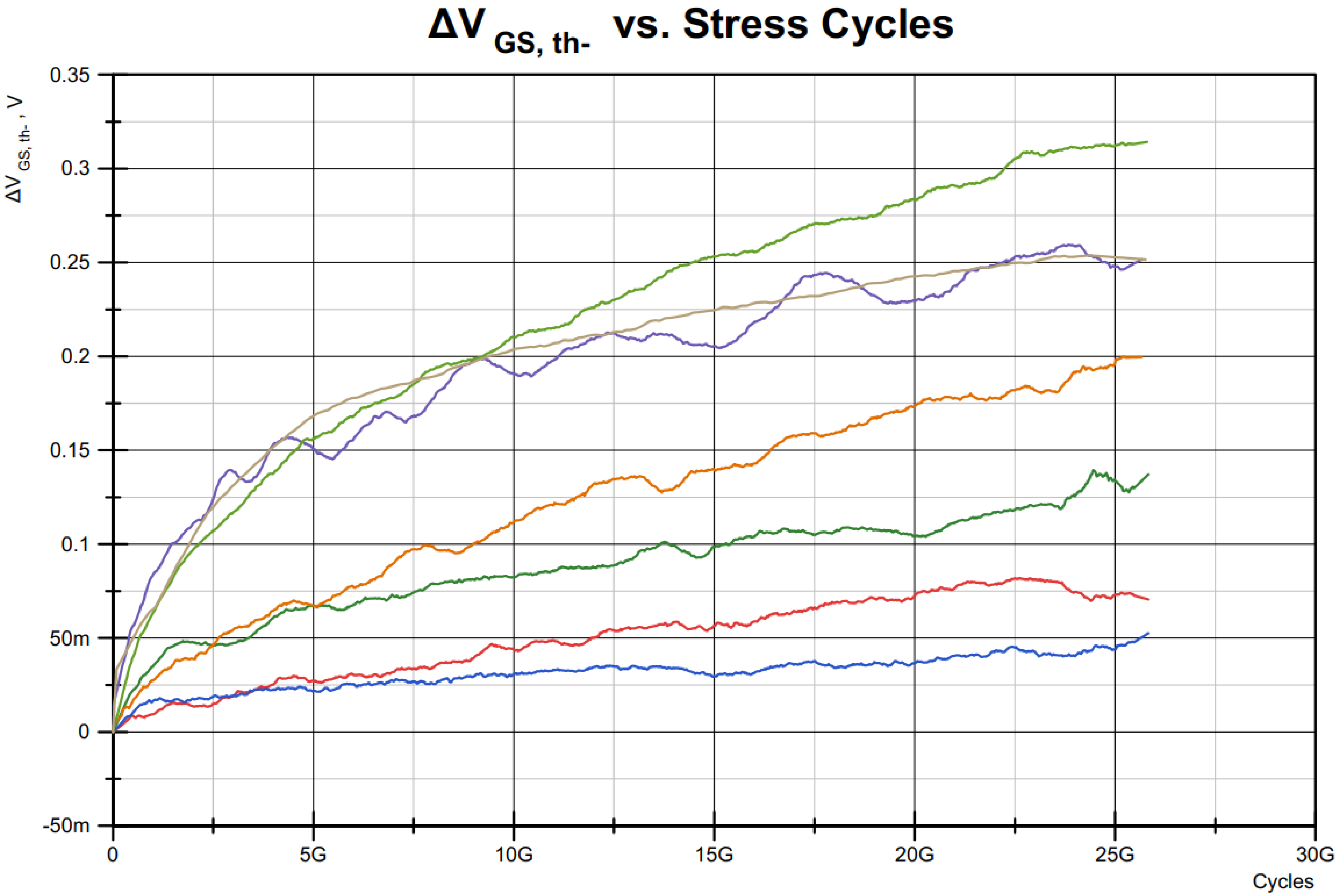
Even tiny ns wide voltage spikes (exp undershoot) can bring a big difference!

DGS/GSS

To get a technology overview, multiple devices from several vendors were used to test the latest generation (available on the market), all …

- 1200 V SiC MOSFET
- 80 mΩ
- latest generation available on the market

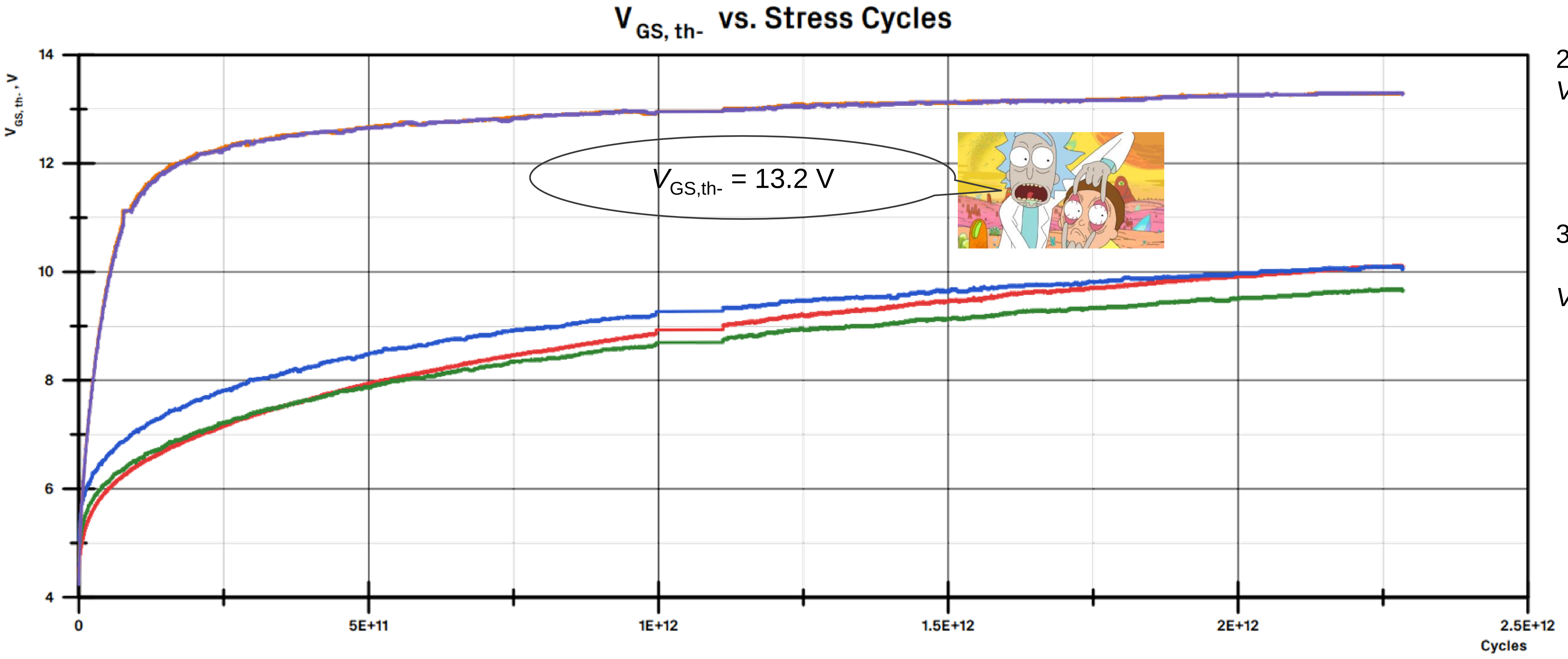
Publicly available Devices, Part A,B,C,D…



- *f*: 100 kHz
- T_c: 25 °C

Overview of available 1200 V, 80 mΩ parts

Publicly available Devices, Part A,B,C,D...


$V_{GS,\,th-}$ vs. Stress Cycles

2 DUTs
$V_{GS,th-}$ = 13.2 V

3 DUTs

$V_{GS,th-}$ ≈ 9.5 V to 10 V

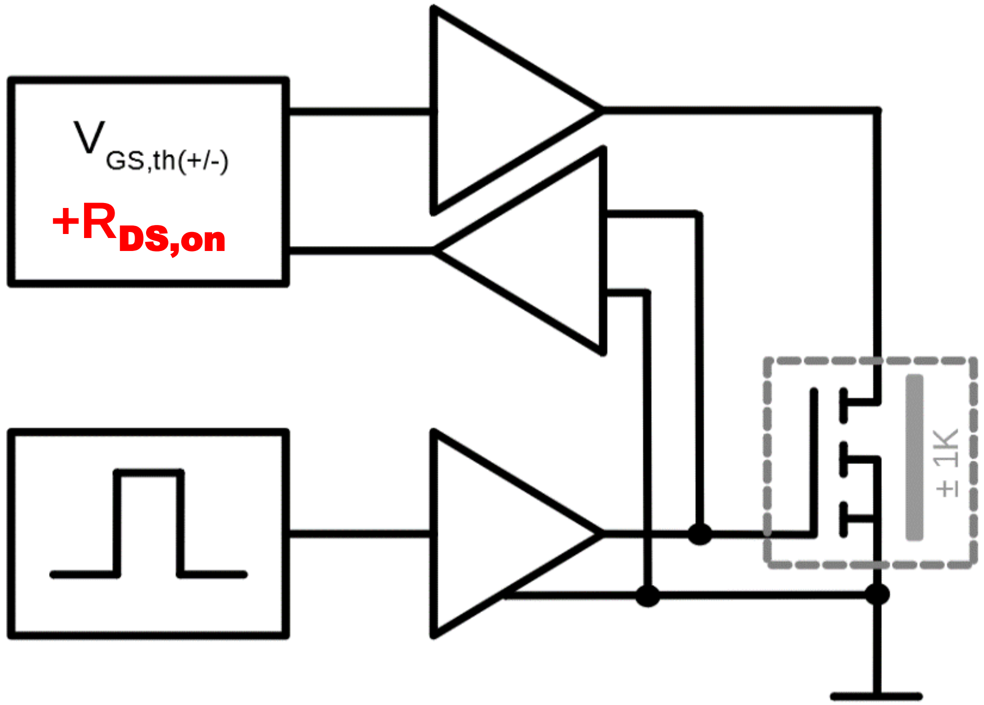
5 parts, same bucket/order from distributor (2023)

$V_{GS,on}$/ $V_{GS,off}$ recommended; 0.6 V/ns; 400 kHz; $2.1\text{x}10^{12}$ cycles; 25°C ... no overstress!

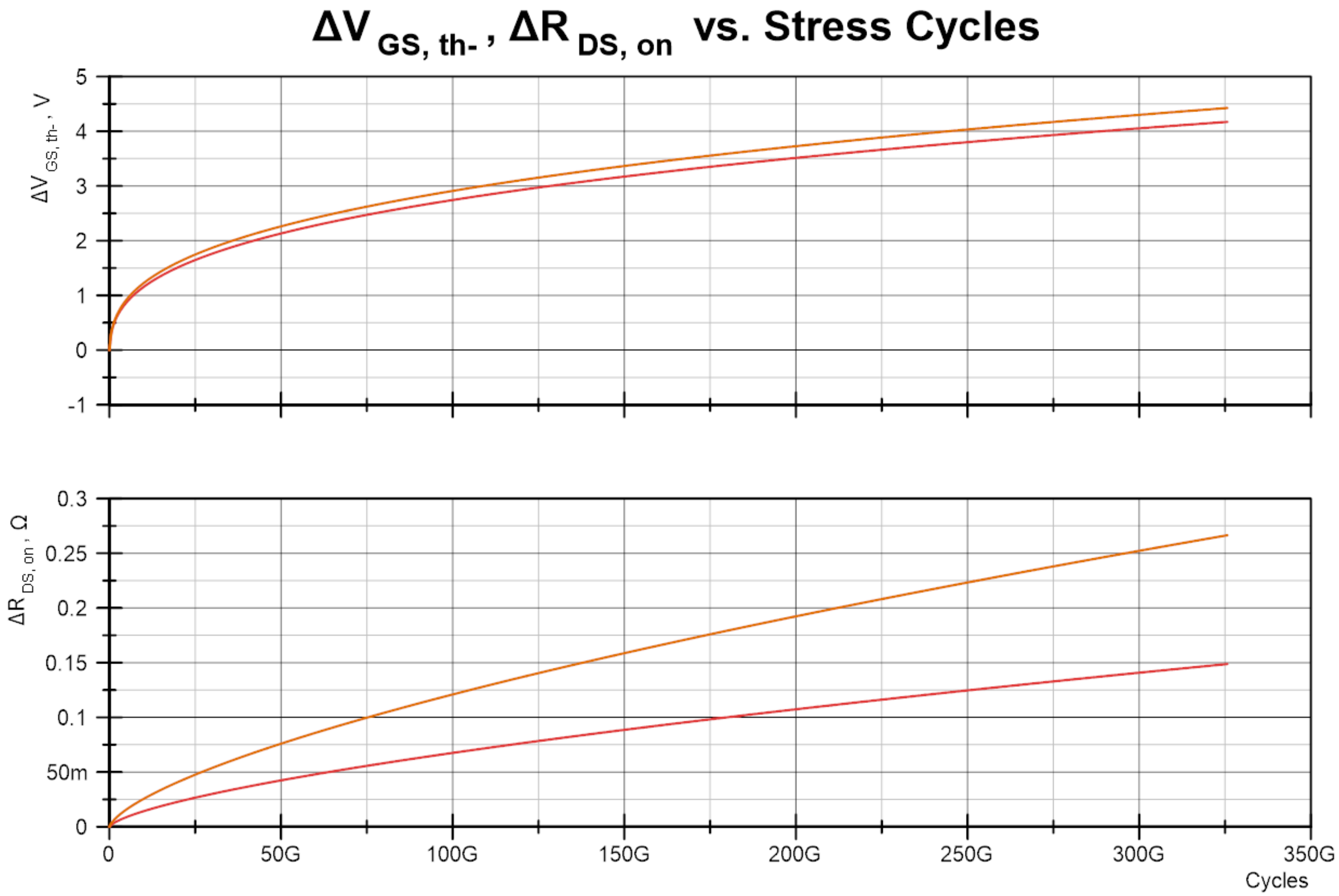
DGS/GSS

- $V_{GS,th}$ drift vs. $R_{DS,on}$ drift: What is the correlation?

- During DGS/GSS Test we monitored in-situ $V_{GS,th\pm}$ and $R_{DS,on}$ as dedicated additional parameter



$V_{GS,th-}$ and $R_{DS,on}$

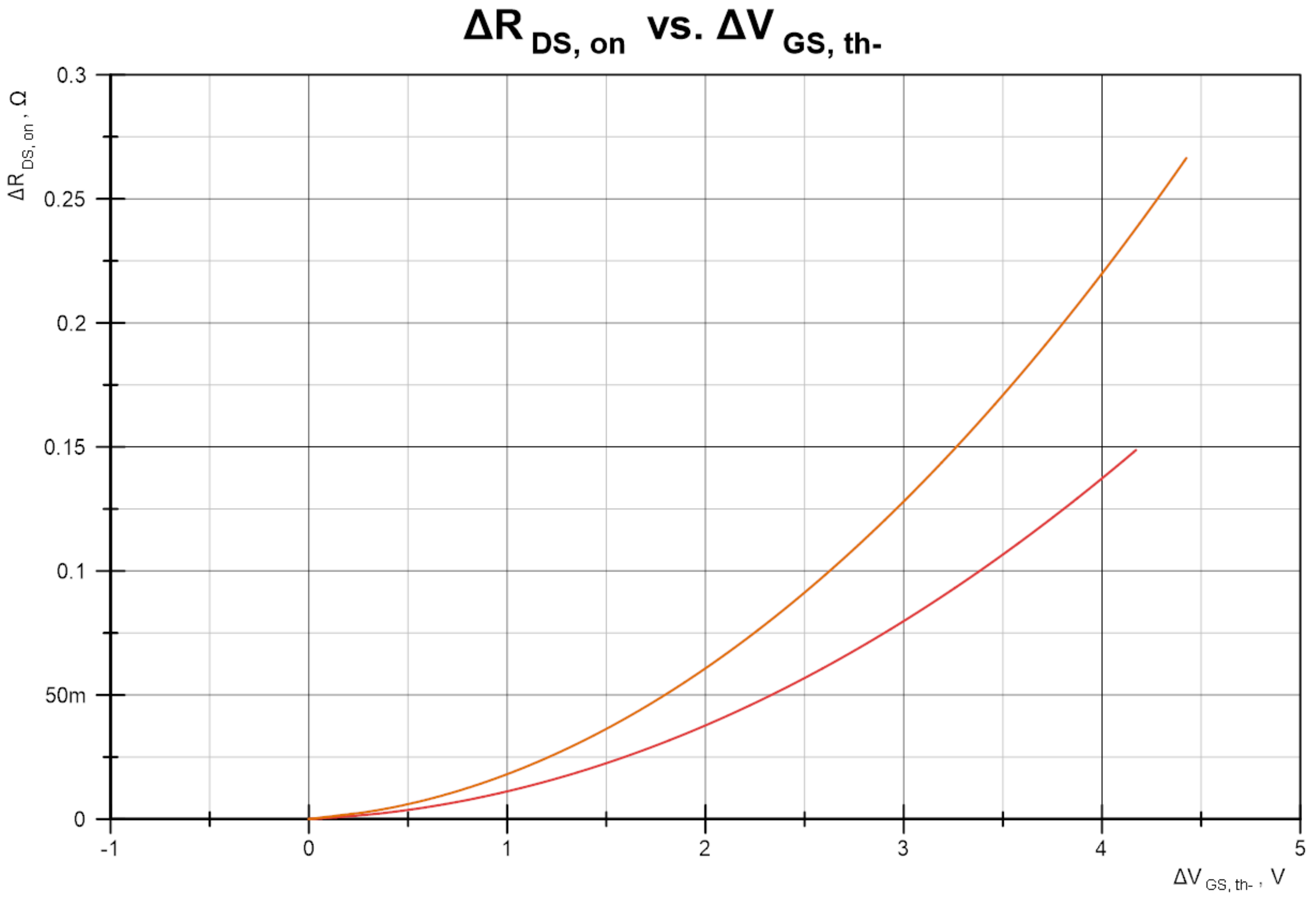


As expected,:
direct relation between
$\Delta V_{GS,th-}$ and $\Delta R_{DS,on}$

3.25×10^{11} cycles
(estimated lifetime of a car
5.76×10^{11} cycles)

$R_{DS,on}$ vs $V_{GS,th-}$

$R_{DS,on}$ drift exponential over $V_{GS,th}$ drift !!



DGS/GSS – long term drift

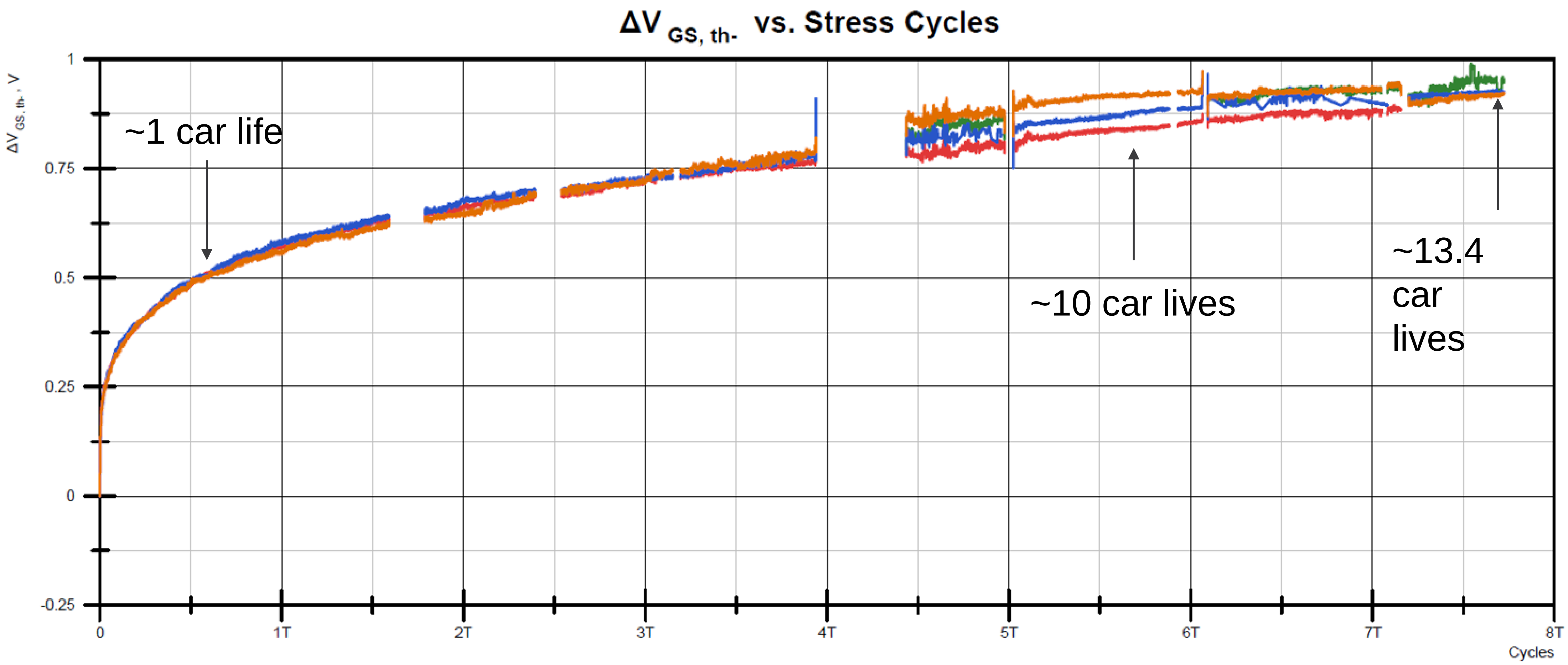
Does the drift end some where?

- Start of test: 2021-12-17
- Date of report: 2023-03-09

- Temperature: 25 °C
- Stress frequency: 400 kHz
- Number of cycles: 7.7×10^{12} cycles / ~13.4 car lives

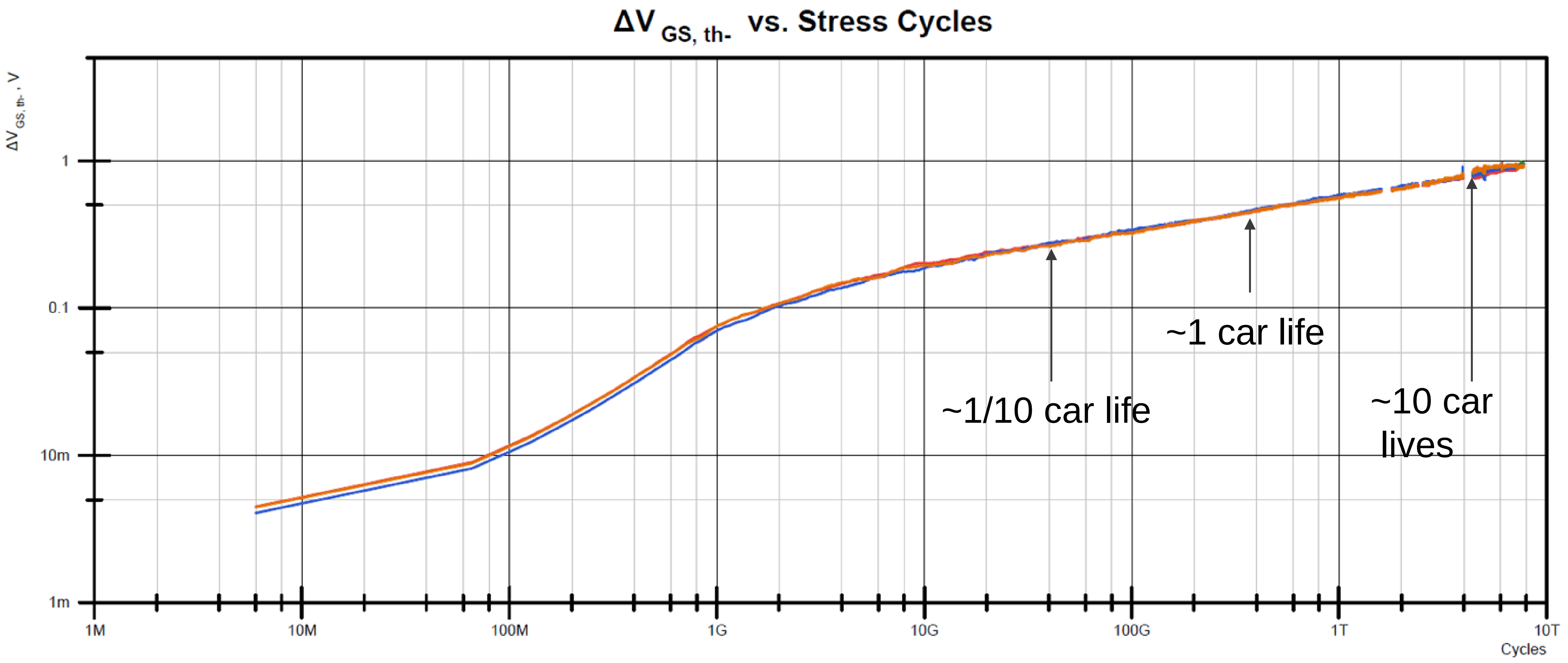
DGS/GSS – long term drift

Does the drift end some where?



DGS/GSS – long term drift

Does the drift end some where?

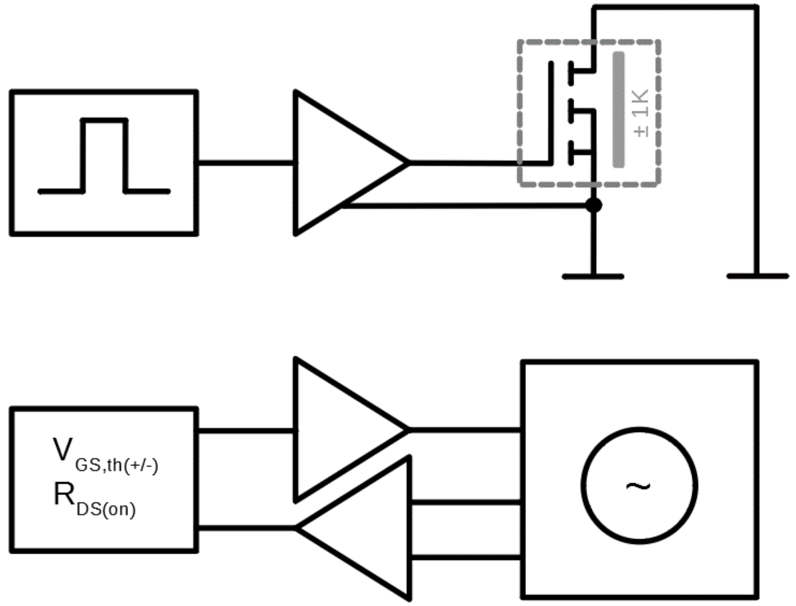


There is no sign of any change in slope visible

In a nutshell – DGS/GSS

Suggested test parameters

Parameter	Value	Remark
Test duration	5.76×10^{11} cycles	Or application specific
Test temperature	25 °C ± 5 K, stability over test ≤ 1 K	ΔT significant
Gate voltage	$V_{GS,max}$; $V_{GS,min}$	No overshoots
Gate frequency	150 kHz to 400 kHz, 50 % DC	Covered acc factors
Gate transient	1 V/ns	No overshoots



Measurement	Readout time	Remark
$V_{GS,th\pm}$	begin, end (minimum) all 5 min (recommended)	const. time < 1 s between stress end and readout
$R_{DS,on}$	begin, end (minimum) all 5 min (recommended)	const. time < 1 s between stress end and readout

Implementing dyn H3TRB

Conventional/static H3TRB:

- Tests the DUT for degradation due to humidity and temperature
- High Voltage is applied

- Typical parameter:

Environment:	85 °C, 85 % rel. Humidity
Voltage:	80 % to 100 % $V_{\mathrm{DS,max}}$ (1 kV to 4 kV)
Time:	1000 h

Quelle: www.infineon.com

Dynamic H3TRB

AQG 324 is first to include dynamic stress in the qualification

Typical values to accelerate the test are:

- Frequency: 100 kHz to 300 kHz (DUT passive)
- Stimuli $\mathrm{d}V/\mathrm{d}t$: 10 V/ns to 100 V/ns, typ. 50 V/ns
- Voltage Stimuli: 50 % to 100 % of $V_{\mathrm{DS,max}}$, typ. 80 % of $V_{\mathrm{DS,max}}$

Additionally, standard conditions are:

- Environment: 85 °C, 85 % relative humidity
- Test time: 1000 h to 2000 h (representing an accelerated car life)

Implementing Dynamic H3TRB/DRB

Experience on implementing dynamic H3TRB/DRB

Data Basis:

- > 45 different setups
  Single chip and modules; diodes and FET; GaN and SiC
- 14 companies
- Present state: ≈ 75 % of setups are DUT active.
  However, trend goes to DUT passive (> 50 % of ordered channels)

Implementing Dynamic H3TRB/DRB

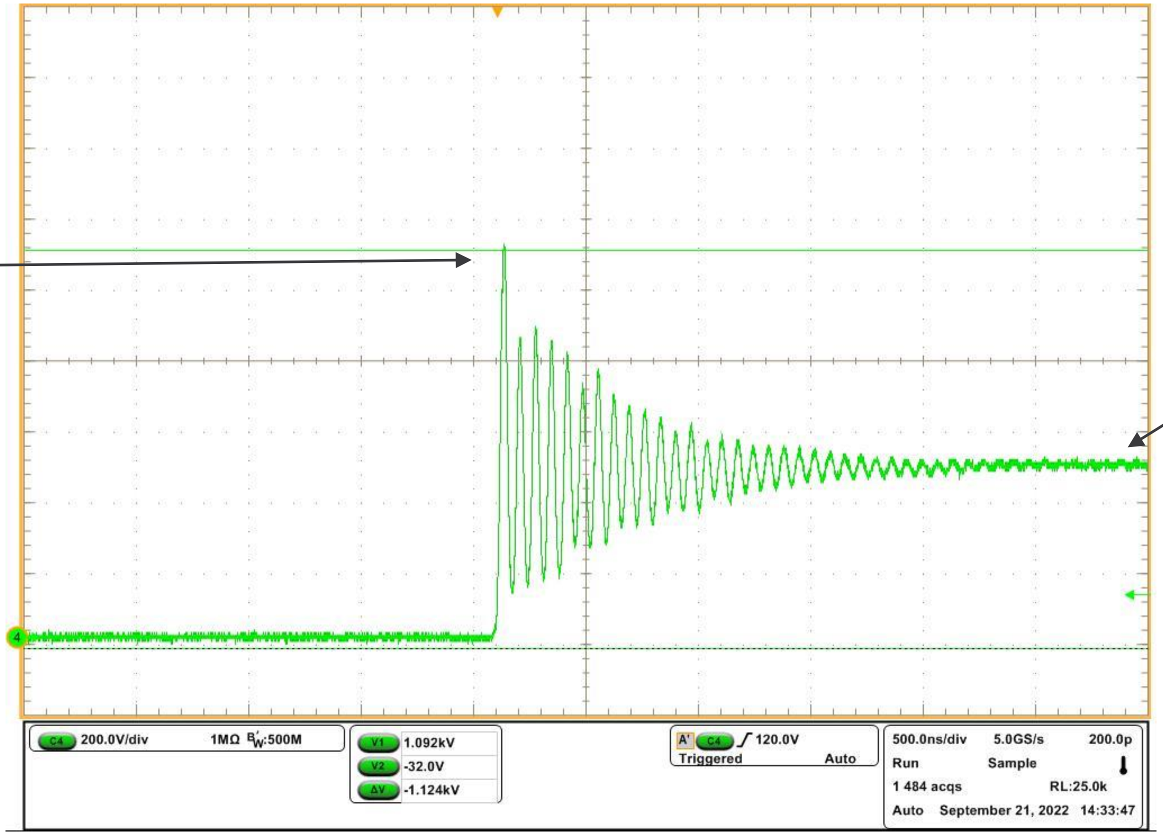
- Curve discussion:
  AQG:
  - Overshoot: 0.8 to 0.95 × $V_{DS,max}$ (DRB & dynamic H3TRB)
  - DC-Voltage: > 0.8 × $V_{DS,max}$ (DRB)
    > 0.5 × $V_{DS,max}$ (dynamic H3TRB)

However, on implementing the curve should be examined

Implementing Dynamic H3TRB/DRB

- Curve discussion:

✓ Peak
0.8 to 0.95 × $V_{DS,max}$



C4 200.0V/div 1MΩ B_W:500M

V1 1.092kV
V2 -32.0V
ΔV -1.124kV

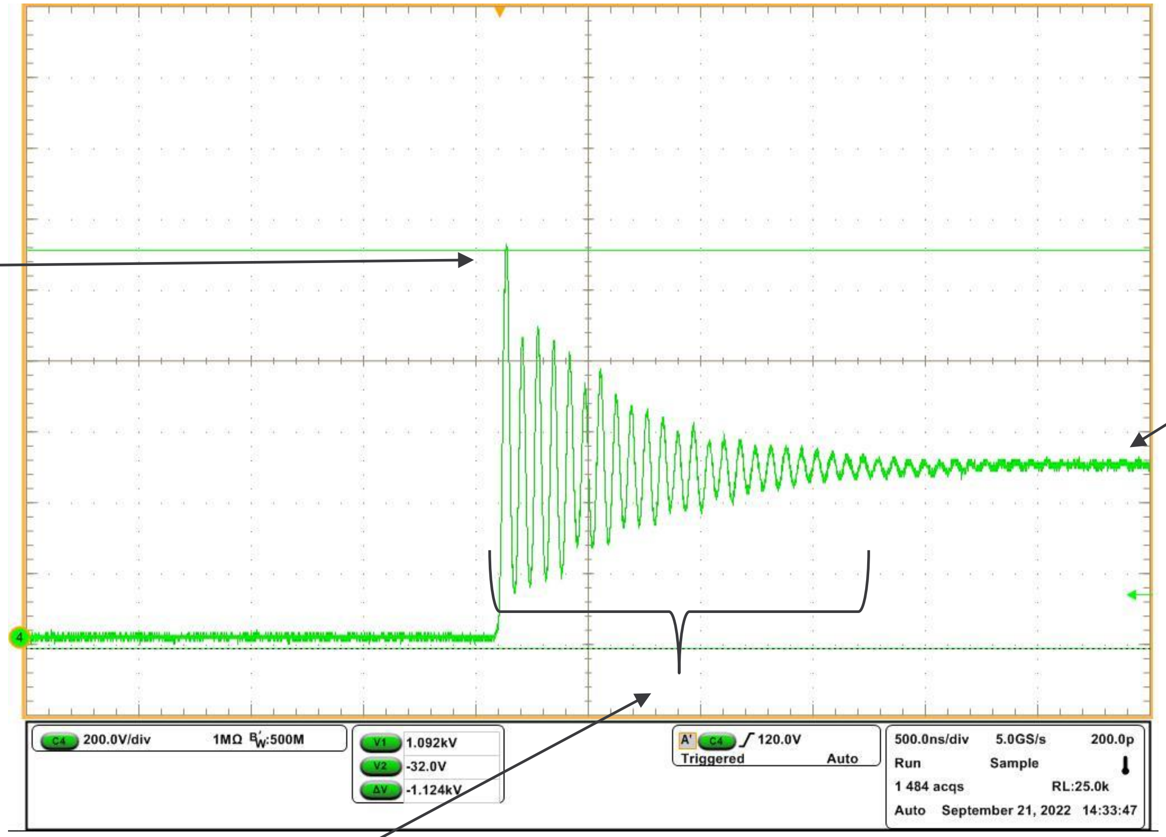
A' C4 ∫ 120.0V
Triggered Auto

500.0ns/div 5.0GS/s 200.0p
Run Sample
1 484 acqs RL:25.0k
Auto September 21, 2022 14:33:47

✓ V_{DS} (for dyn. H3TRB)
> 0.5 × $V_{DS,max}$

Implementing Dynamic H3TRB/DRB

- Curve discussion:



✓ Peak
0.8 to 0.95 × $V_{\mathrm{DS,max}}$

✓ V_{DS} (for dyn. H3TRB)
> 0.5 × $V_{\mathrm{DS,max}}$

Influence of high Oscillation?

- Accelerating as multiple cycles?
- Deaccelerating due to „preventing“ effect by directly reversing dV/dt slope?

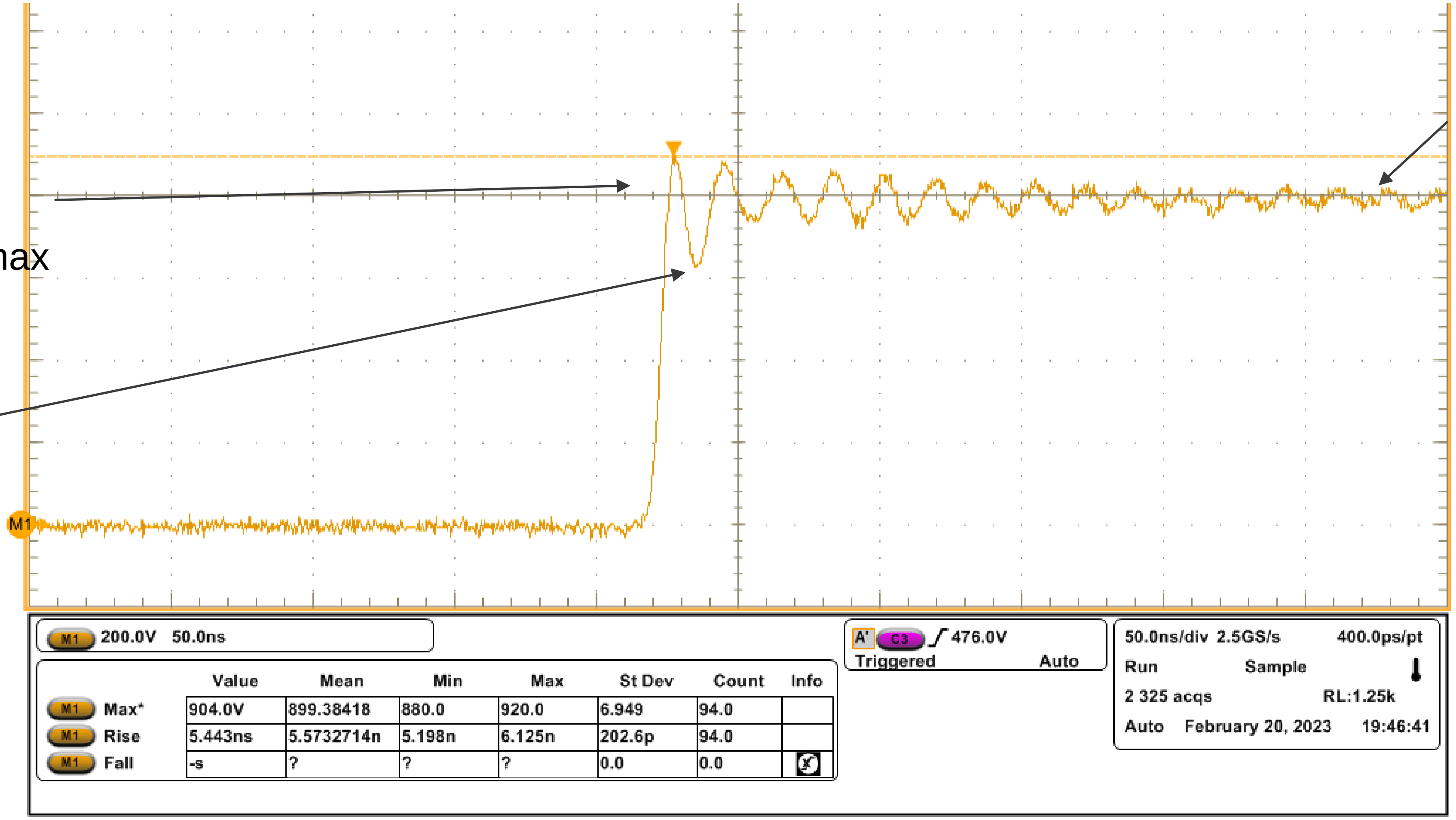
Implementing Dynamic H3TRB/DRB

- Overshoot: 0.8 to 0.95 × $V_{DS,max}$ (DRB & dynamic H3TRB)
- V_{Stress} : > 0.8 × $V_{DS,max}$ (DRB) / > 0.5 × $V_{DS,max}$ (dynamic H3TRB)
- 1st minima > 0.5 × V_{Stress}

✓ Peak
0.8 to 0.95 × $V_{DS,max}$

✓ 1st minima
> 0.5 x V_{Stress}

✓ V_{DS}
>0.8 × $V_{DS,max}$



M1 200.0V 50.0ns

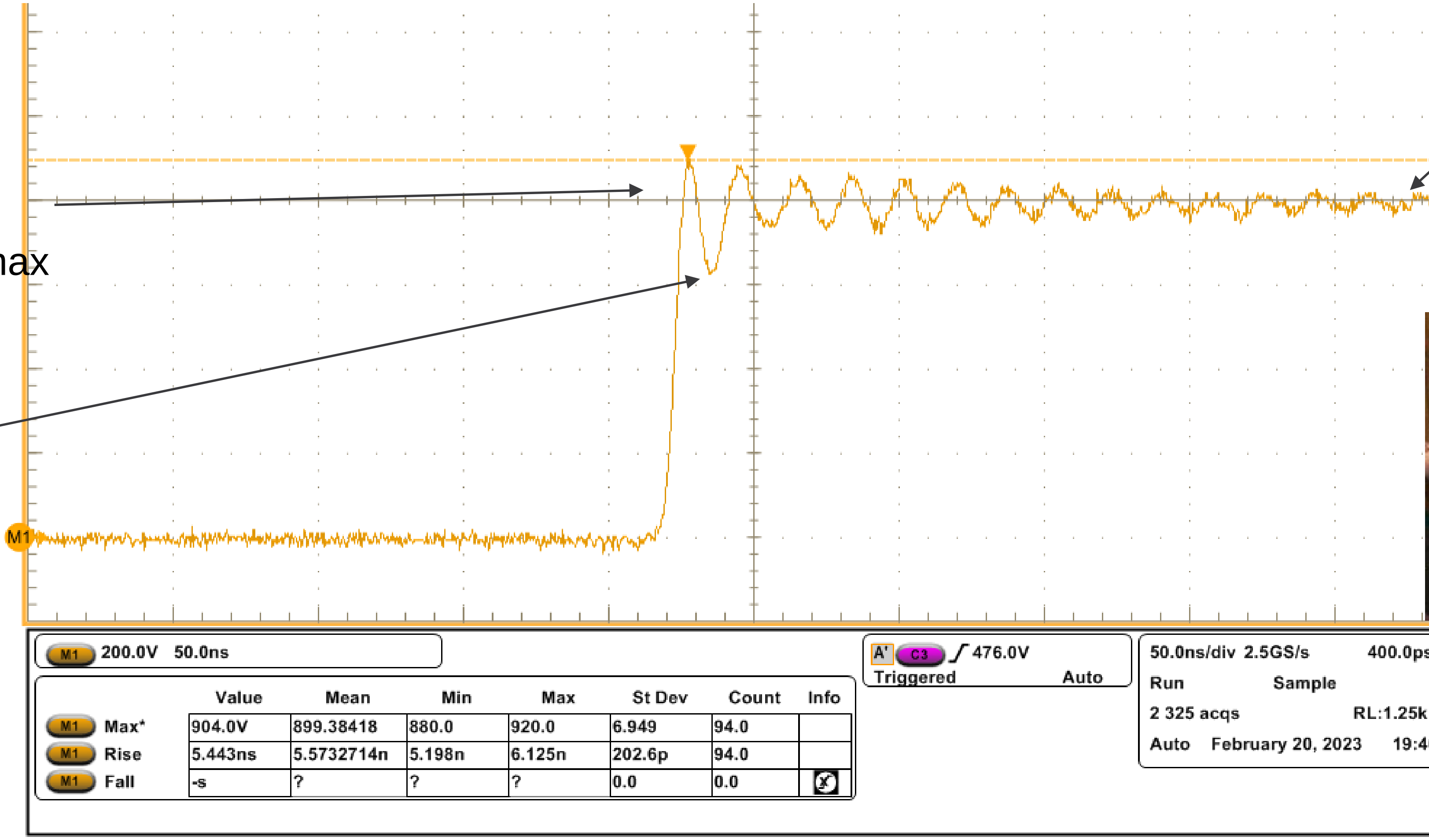
	Value	Mean	Min	Max	St Dev	Count	Info
M1 Max*	904.0V	899.38418	880.0	920.0	6.949	94.0	
M1 Rise	5.443ns	5.5732714n	5.198n	6.125n	202.6p	94.0	
M1 Fall	-s	?	?	?	0.0	0.0	☒

A' C3 ⎰ 476.0V
Triggered Auto

50.0ns/div 2.5GS/s 400.0ps/pt
Run Sample
2 325 acqs RL:1.25k
Auto February 20, 2023 19:46:41

Implementing Dynamic H3TRB/DRB

- Overshoot: 0.8 to 0.95 × $V_{\mathrm{DS,max}}$ (DRB & dynamic H3TRB)
- V_{Stress} : > 0.8 × $V_{\mathrm{DS,max}}$ (DRB) / > 0.5 × $V_{\mathrm{DS,max}}$ (dynamic H3TRB)
- 1st minima > 0.5 × V_{Stress}



✓ Peak
0.8 to 0.95 × $V_{\mathrm{DS,max}}$

✓ 1st minima
> 0.5 × V_{Stress}

✓ V_{DS}
>0.8 × $V_{\mathrm{DS,max}}$

M1 200.0V 50.0ns

	Value	Mean	Min	Max	St Dev	Count	Info
M1 Max*	904.0V	899.38418	880.0	920.0	6.949	94.0	
M1 Rise	5.443ns	5.5732714n	5.198n	6.125n	202.6p	94.0	
M1 Fall	-s	?	?	?	0.0	0.0	ⓧ

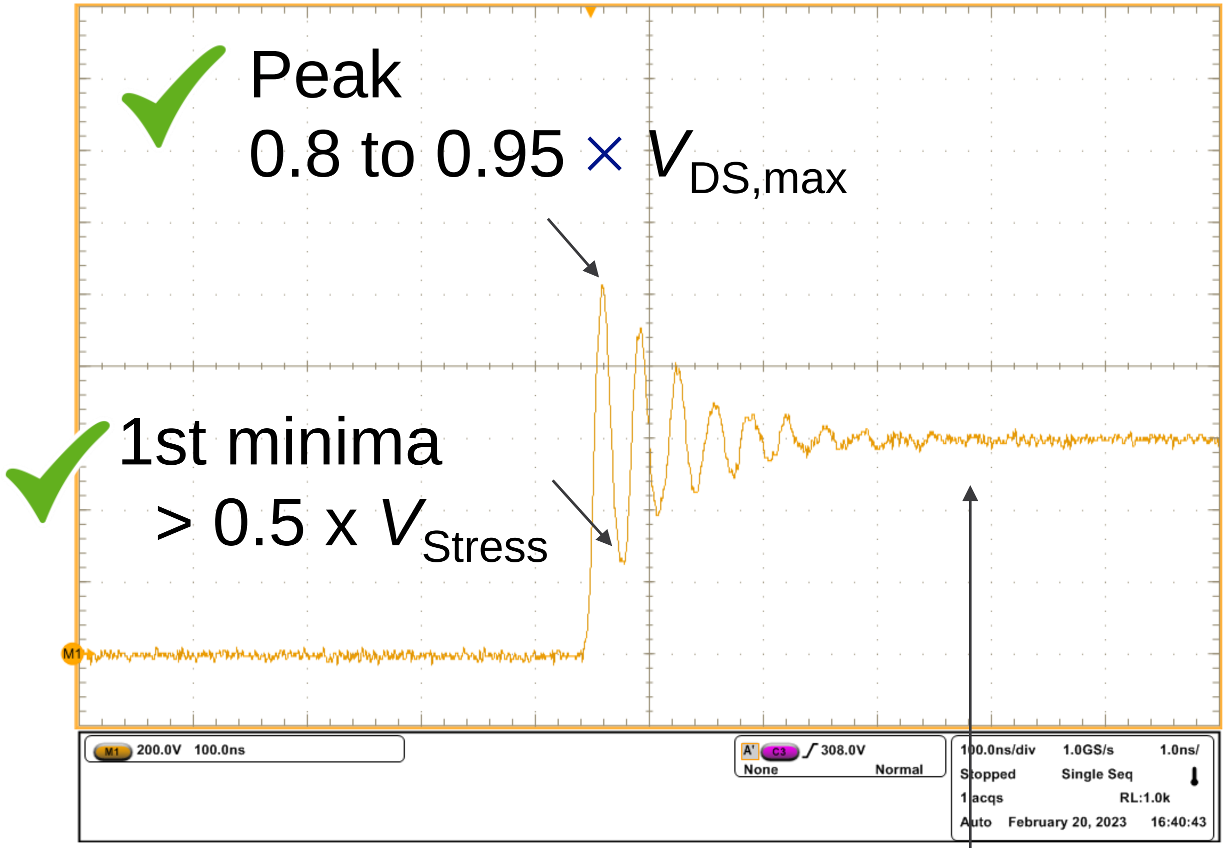
A' C3 ∫ 476.0V
Triggered Auto

50.0ns/div 2.5GS/s 400.0ps/pt
Run Sample
2 325 acqs RL:1.25k
Auto February 20, 2023 19:46:41

Implementing Dynamic H3TRB/DRB

- How to measure dV/dt ?

  (examples that barely pass)

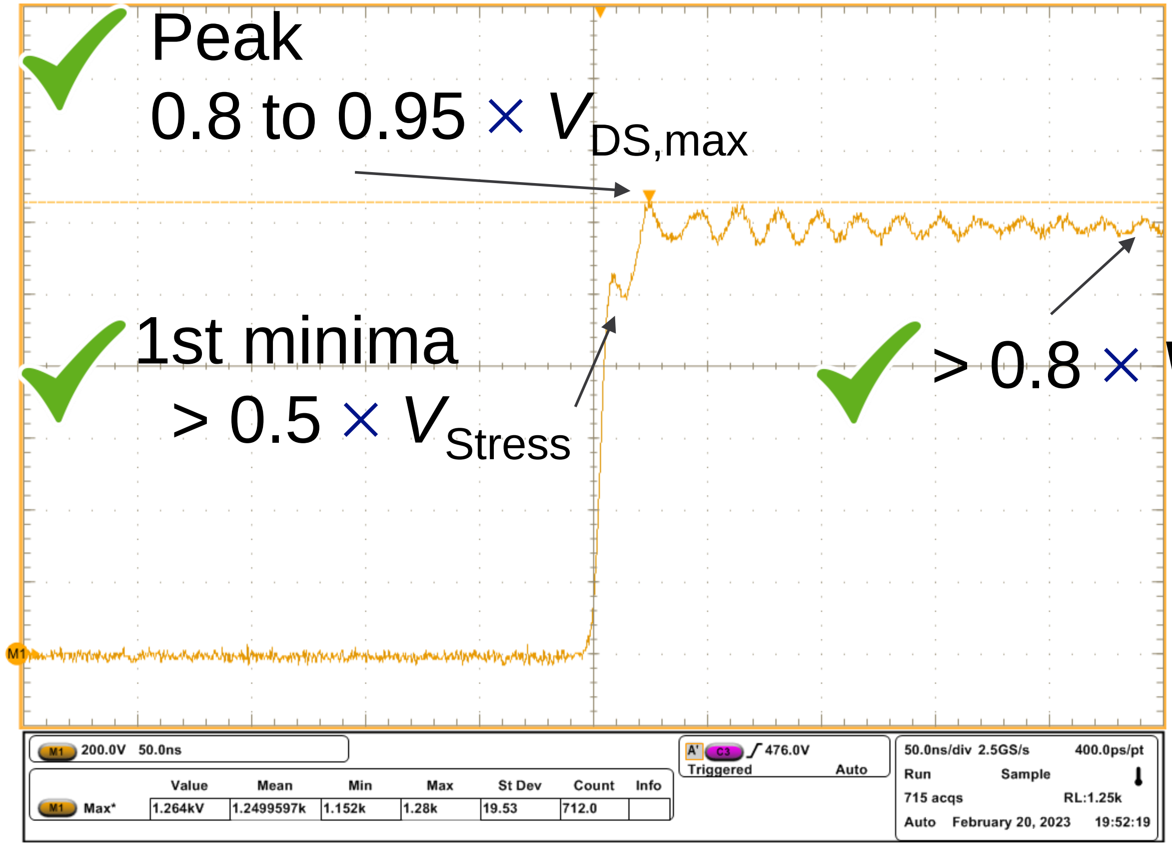


✓ Peak

0.8 to 0.95 × $V_{DS,max}$

✓ 1st minima

> 0.5 x V_{Stress}



✓ Peak

0.8 to 0.95 × $V_{DS,max}$

✓ 1st minima

> 0.5 × V_{Stress}

✓ > 0.8 × $V_{DS,max}$

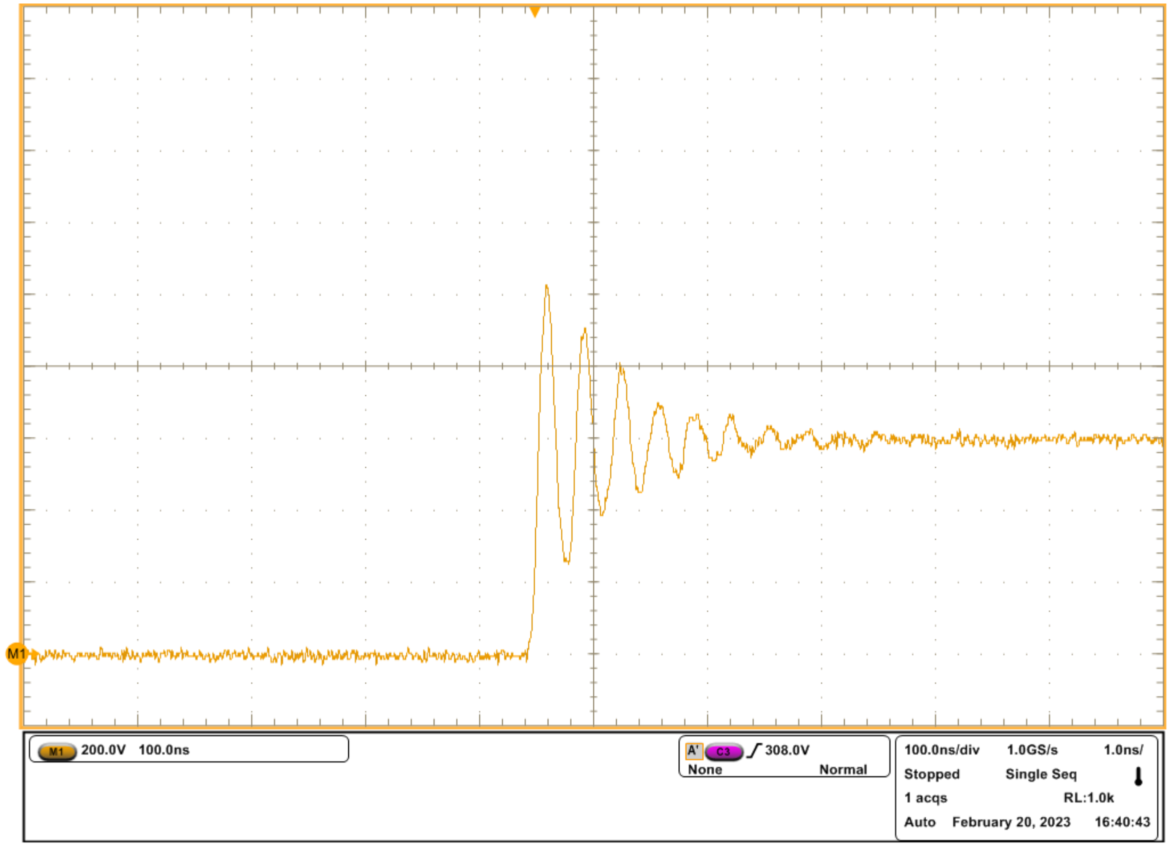
	Value	Mean	Min	Max	St Dev	Count	Info
M1 Max*	1.264kV	1.2499597k	1.152k	1.28k	19.53	712.0	

✓ Dyn. H3TRB (> 0.5 x $V_{DS,max}$)

✗ DRB (> 0.8 x $V_{DS,max}$)

Implementing Dynamic H3TRB/DRB

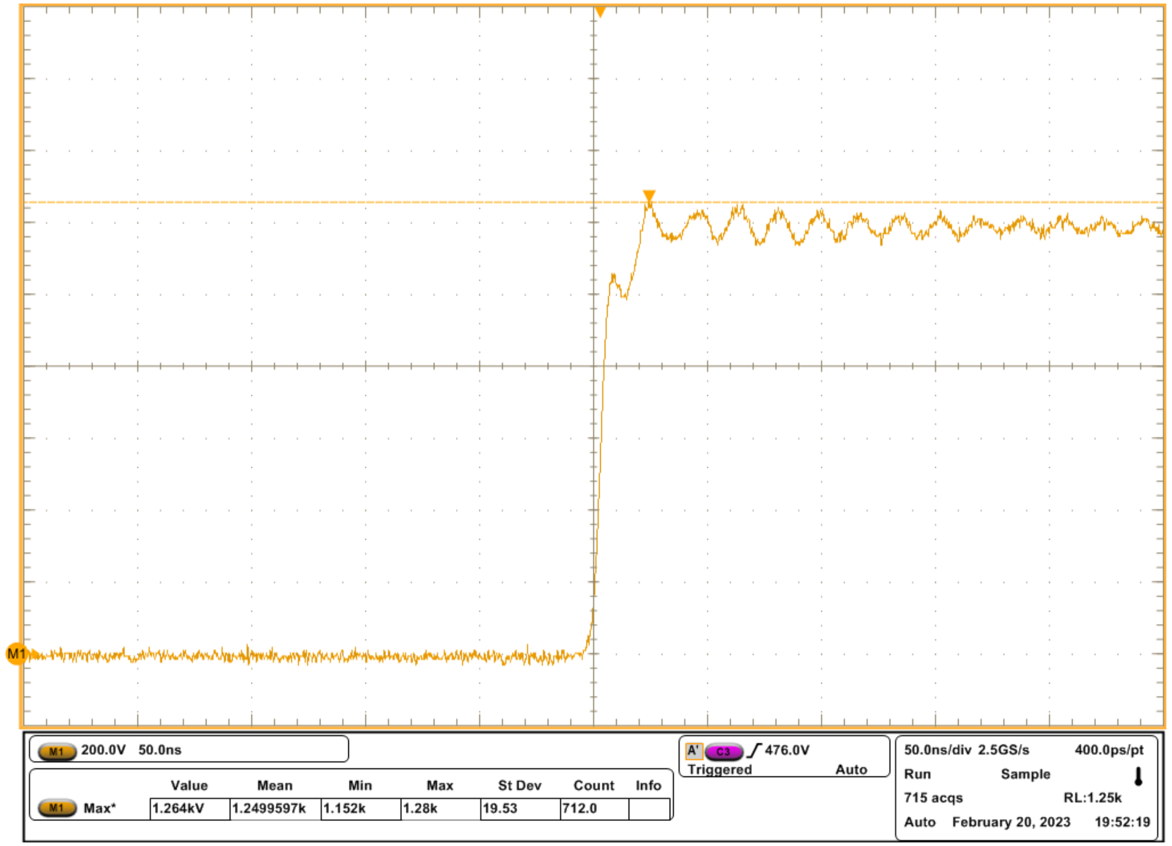
- How to measure d*V*/d*t* ?



M1 200.0V 100.0ns

A' C3 308.0V
None Normal

100.0ns/div 1.0GS/s 1.0ns/
Stopped Single Seq
1 acqs RL:1.0k
Auto February 20, 2023 16:40:43



M1 200.0V 50.0ns

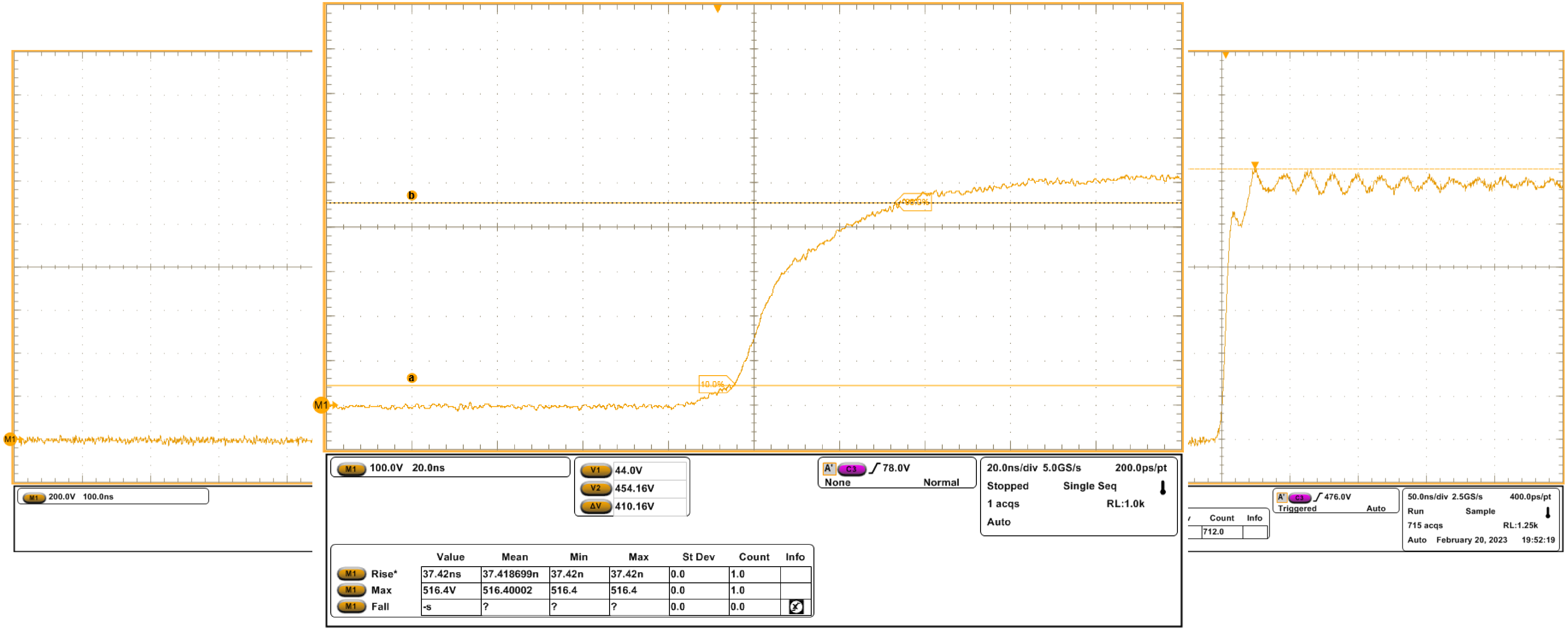
	Value	Mean	Min	Max	St Dev	Count	Info
M1 Max*	1.264kV	1.2499597k	1.152k	1.28k	19.53	712.0	

A' C3 476.0V
Triggered Auto

50.0ns/div 2.5GS/s 400.0ps/pt
Run Sample
715 acqs RL:1.25k
Auto February 20, 2023 19:52:19

Implementing Dynamic H3TRB/DRB

- How to measure d*V*/d*t* ?



M1 200.0V 100.0ns

M1 100.0V 20.0ns

V1 44.0V
V2 454.16V
ΔV 410.16V

A' C3 ∫ 78.0V
None Normal

20.0ns/div 5.0GS/s 200.0ps/pt
Stopped Single Seq
1 acqs RL:1.0k
Auto

	Value	Mean	Min	Max	St Dev	Count	Info
M1 Rise*	37.42ns	37.418699n	37.42n	37.42n	0.0	1.0	
M1 Max	516.4V	516.40002	516.4	516.4	0.0	1.0	
M1 Fall	-s	?	?	?	0.0	0.0	☒

Count	Info
712.0	

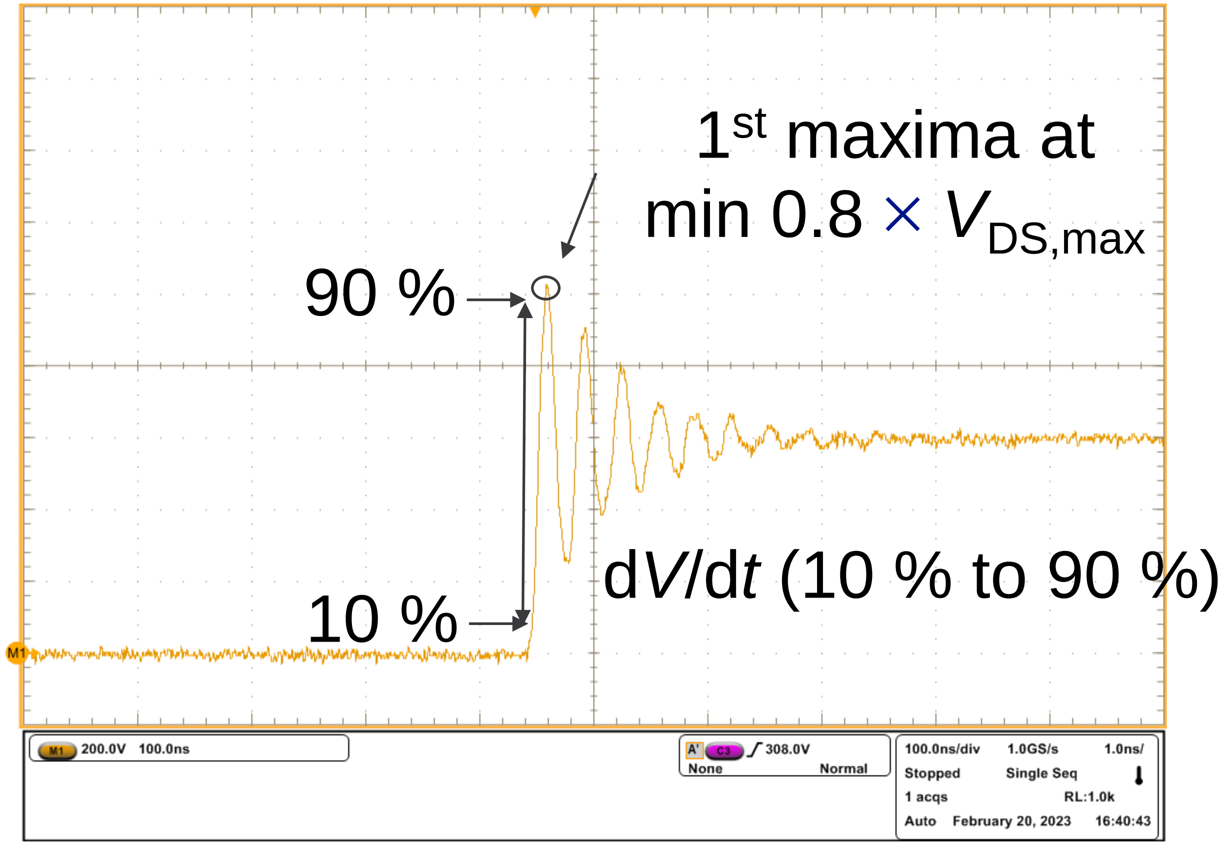
A' C3 ∫ 476.0V
Triggered Auto

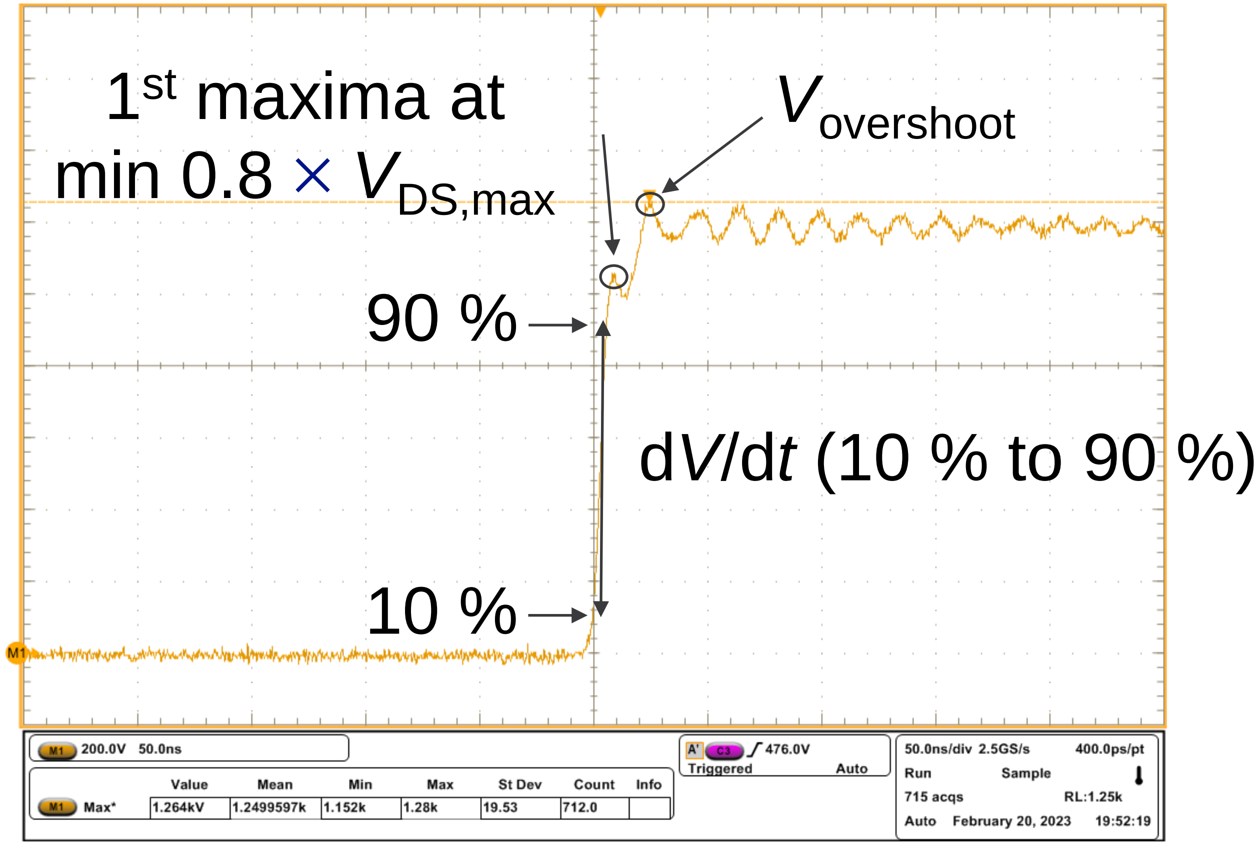
50.0ns/div 2.5GS/s 400.0ps/pt
Run Sample
715 acqs RL:1.25k
Auto February 20, 2023 19:52:19

Implementing Dynamic H3TRB/DRB

Set of guidelines for d*V*/d*t* :

- Measure from min 10 % to max 90 % (or 20/80) of first maxima at min 0.8 × $V_{\mathrm{DS,max}}$
- For non uniform slope less than 90 % is allowed if max > 0.8 × $V_{\mathrm{DS,max}}$





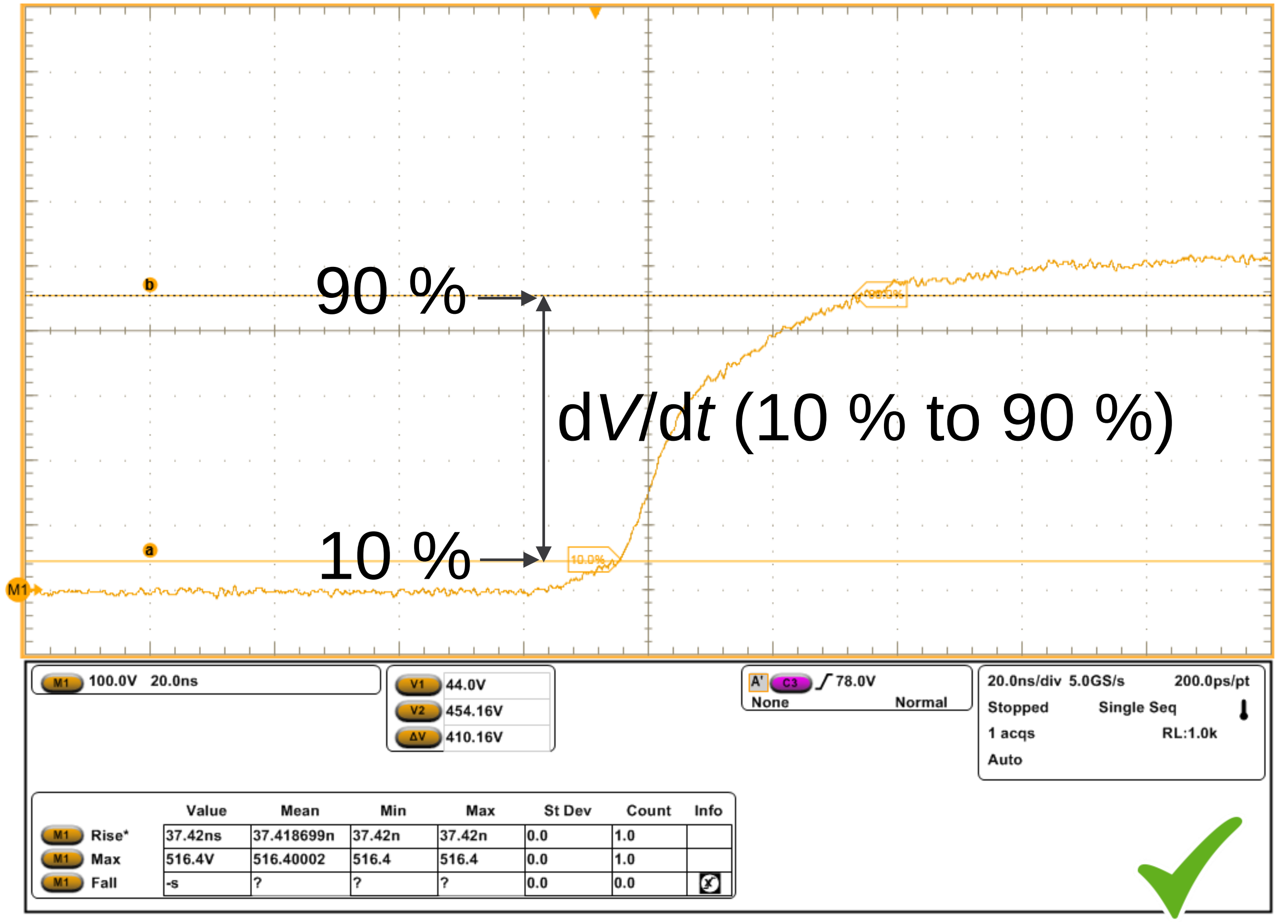
	Value	Mean	Min	Max	St Dev	Count	Info
M1 Max*	1.264kV	1.2499597k	1.152k	1.28k	19.53	712.0	

Note: d*V*/d*t* max is 1st maxima ≠ $V_{\mathrm{overshoot}}$

Implementing Dynamic H3TRB/DRB

Set of guidelines for d*V*/d*t* :

- Measure from min 10 % to max 90 % (or 20/80) of first maxima at min 0.8 × $V_{\mathrm{DS,max}}$
- For non uniform slope less than 90 % is allowed if max > 0.8 × $V_{\mathrm{DS,max}}$



90 %

10 %

d*V*/d*t* (10 % to 90 %)

M1 100.0V 20.0ns

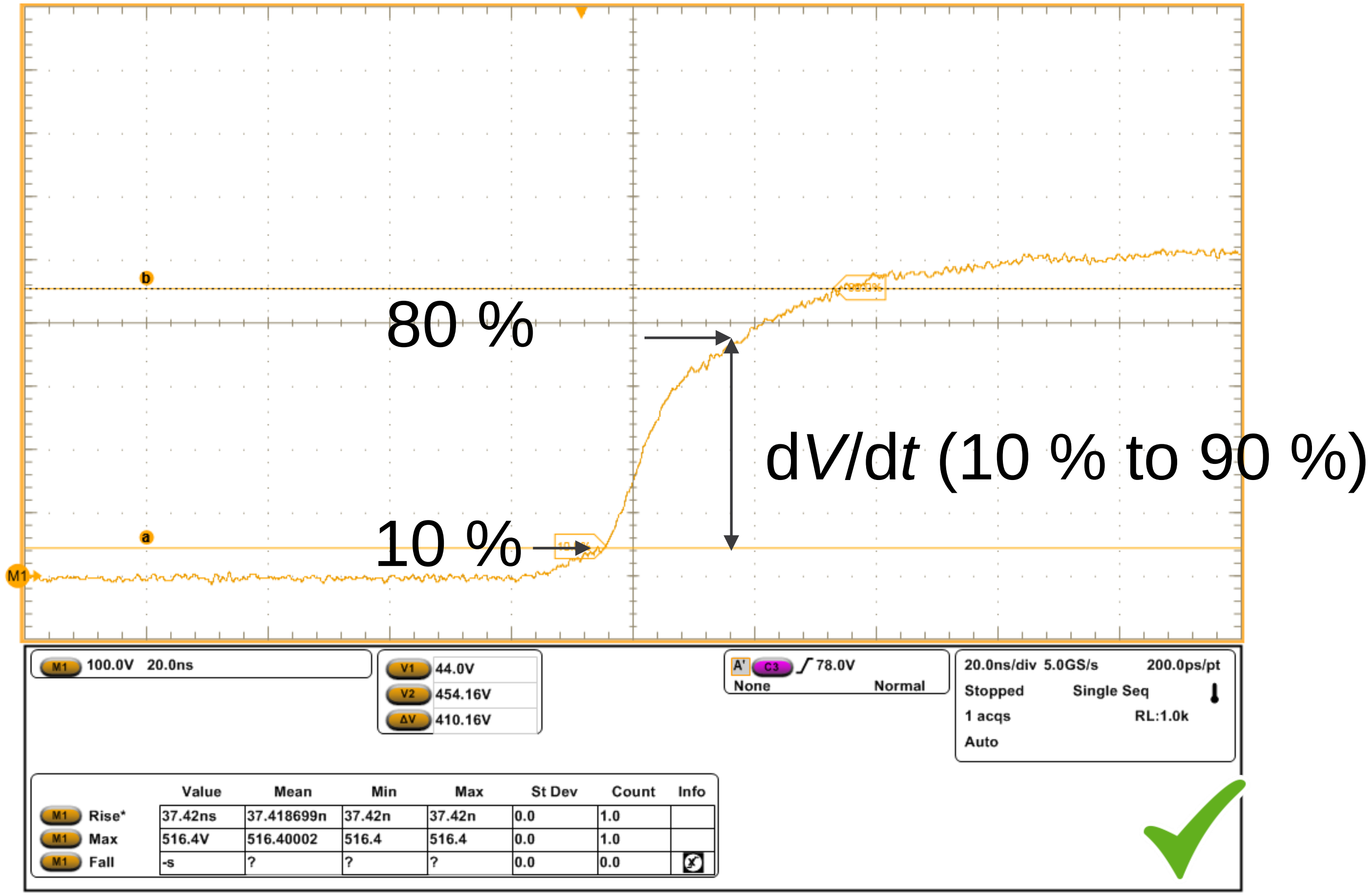
V1 44.0V
V2 454.16V
ΔV 410.16V

A' C3 78.0V
None Normal

20.0ns/div 5.0GS/s 200.0ps/pt
Stopped Single Seq
1 acqs RL:1.0k
Auto

	Value	Mean	Min	Max	St Dev	Count	Info
M1 Rise*	37.42ns	37.418699n	37.42n	37.42n	0.0	1.0	
M1 Max	516.4V	516.40002	516.4	516.4	0.0	1.0	
M1 Fall	-s	?	?	?	0.0	0.0	

✓



80 %

10 %

d*V*/d*t* (10 % to 90 %)

M1 100.0V 20.0ns

V1 44.0V
V2 454.16V
ΔV 410.16V

A' C3 78.0V
None Normal

20.0ns/div 5.0GS/s 200.0ps/pt
Stopped Single Seq
1 acqs RL:1.0k
Auto

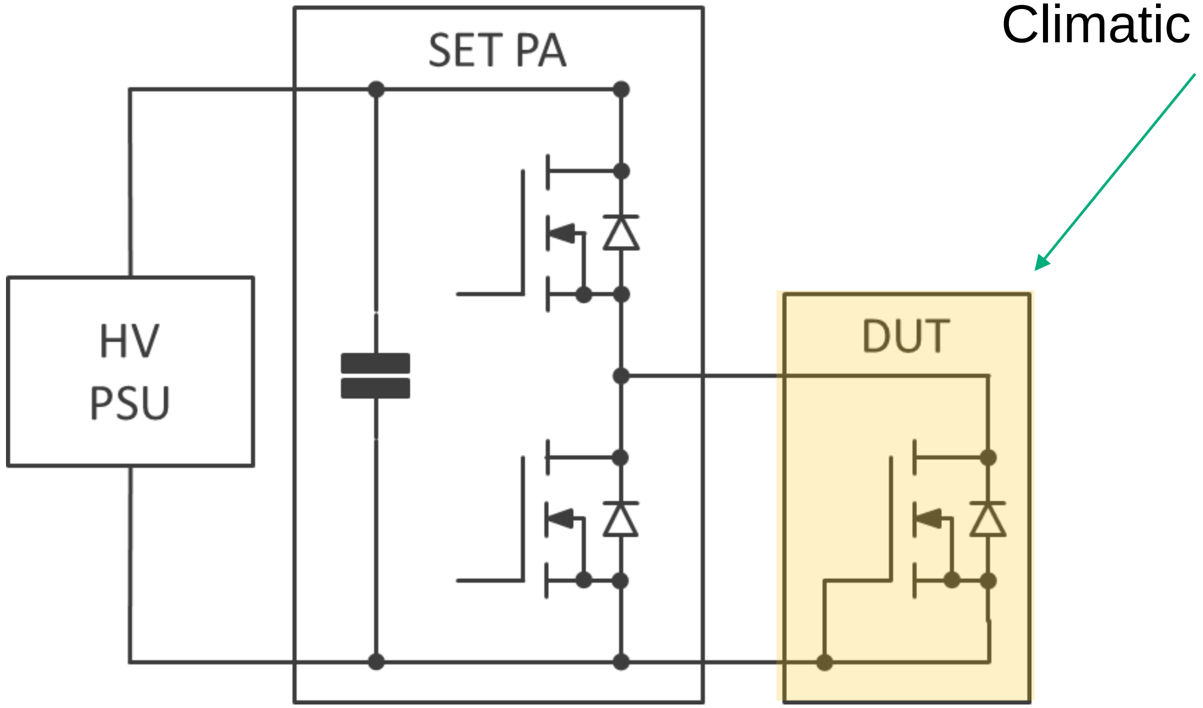
	Value	Mean	Min	Max	St Dev	Count	Info
M1 Rise*	37.42ns	37.418699n	37.42n	37.42n	0.0	1.0	
M1 Max	516.4V	516.40002	516.4	516.4	0.0	1.0	
M1 Fall	-s	?	?	?	0.0	0.0	

✓

Implementing Dynamic H3TRB/DRB

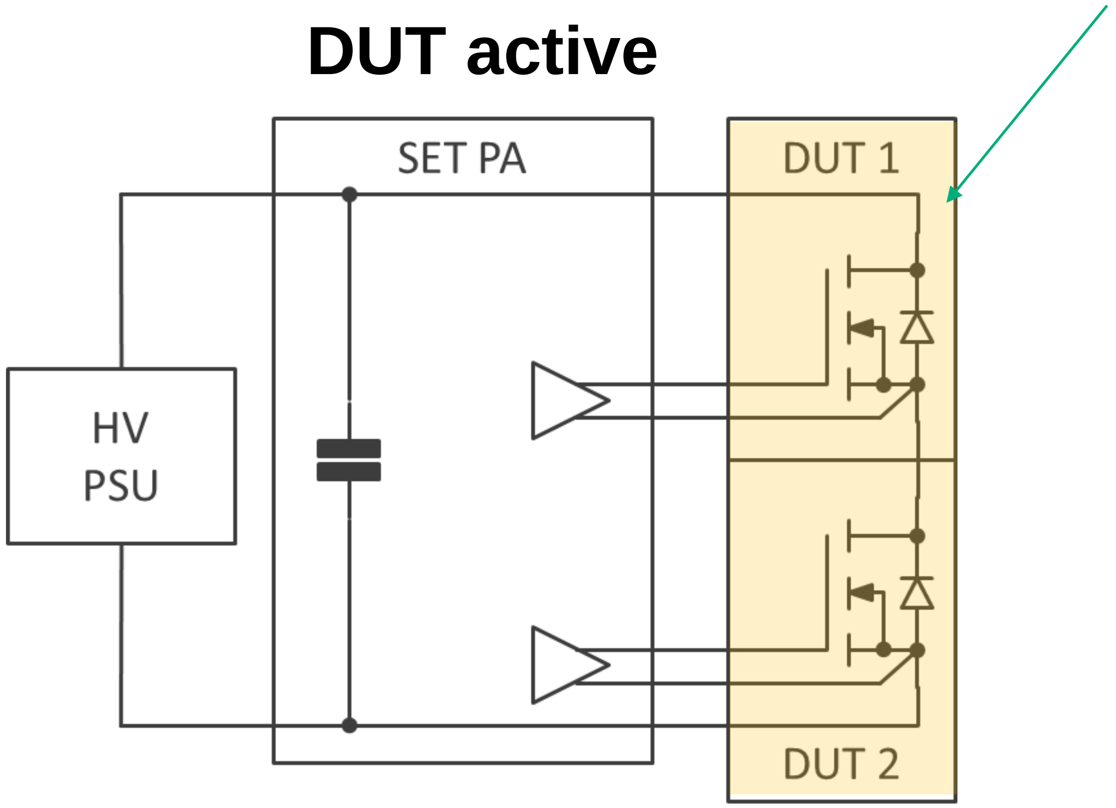
- ~ 75 % DUT active, however trend goes to DUT passive
  (> 50 % of channels in order are DUT passive)

DUT passive



Climatic chamber

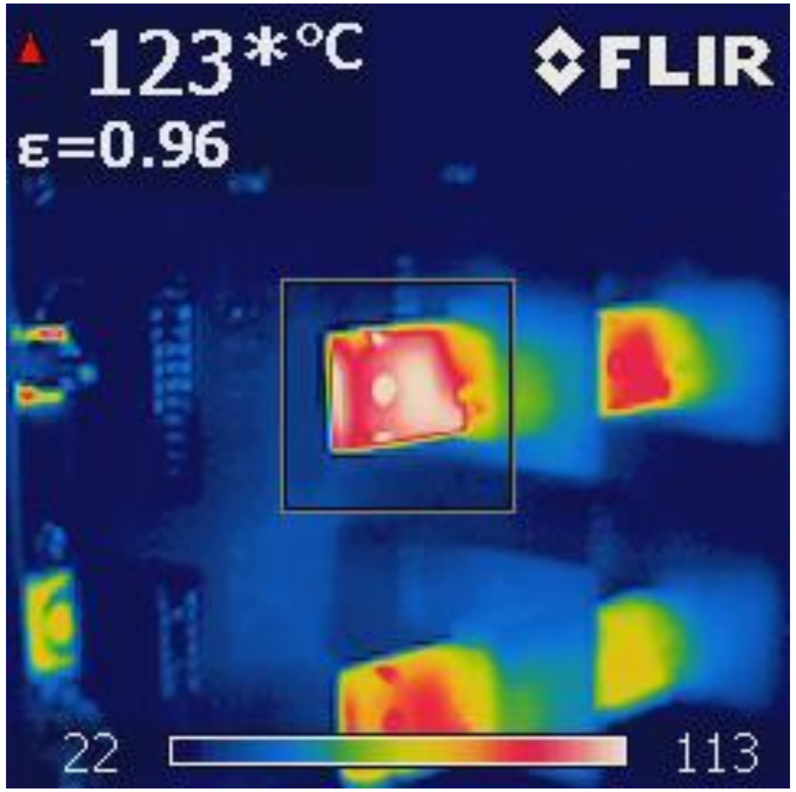
DUT active



Climatic chamber

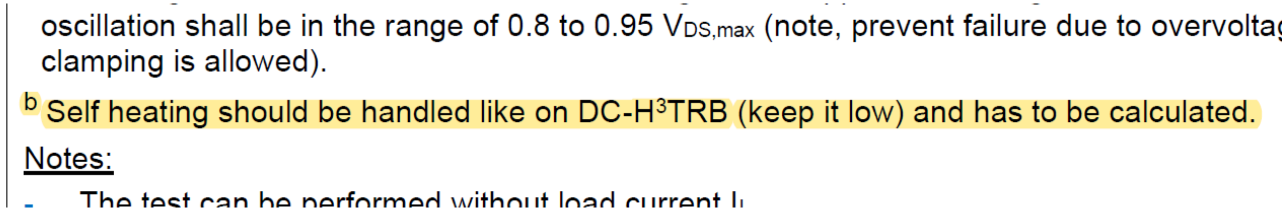
Dynamic H3TRB/DRB in reallife

- Main point for trend :
  DUT heating: limits max frequency for DRB & limit heating for dynamic H3TRB,
  (example: ≈ 4 W/DUT at 15 kHz, for TO 247, $\Delta T_{j-a} = 4\,\mathrm{W} * 20\,\frac{\mathrm{K}}{\mathrm{W}} = 60\,\mathrm{K}$)



Complete energy goes into device,
limits max frequency for DRB not unusual to be < 50 kHz,

For dynamic H3TRB self heating is considerable at 15 kHz,
AQG rightfully states that:



oscillation shall be in the range of 0.8 to 0.95 $V_{DS,max}$ (note, prevent failure due to overvoltag
clamping is allowed).

[b] Self heating should be handled like on DC-H^3TRB (keep it low) and has to be calculated.

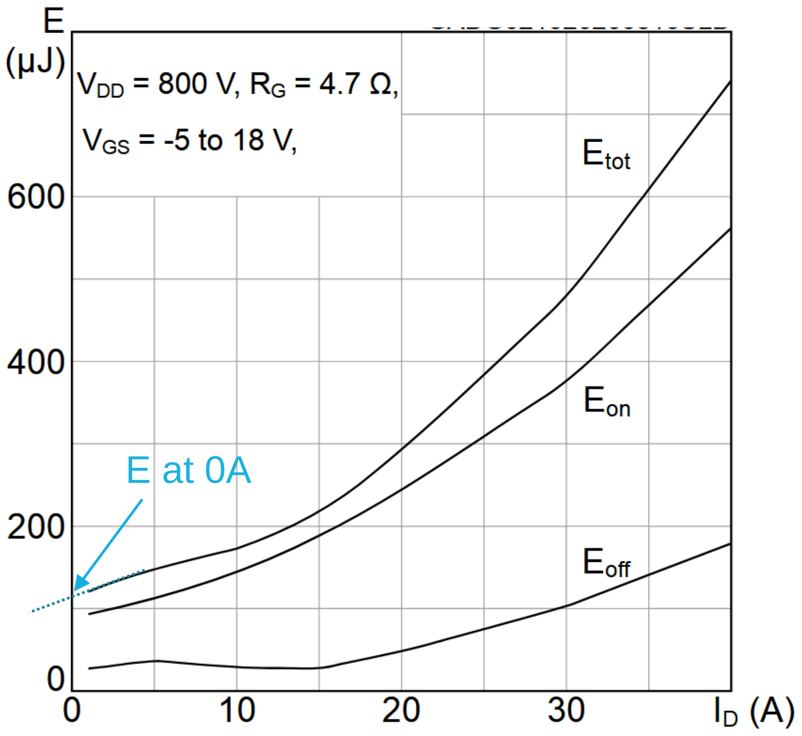
Notes:

- The test can be performed without load current I

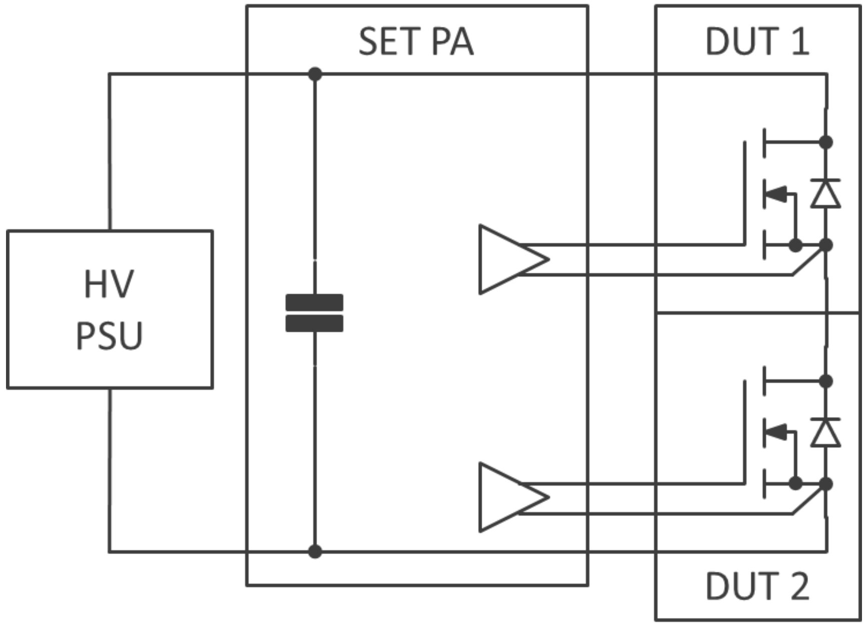
which is often in single digit range (T_c - T_a)
for static H3TRB

Dynamic H3TRB/DRB in reallife

- Calculate losses: don‘t do my mistake:
  $P \neq f_{\text{stress}} * \frac{1}{2} C V^2$, C is nonlinear, ($\int_0^Q V(q)\mathrm{d}q$, voltage per charge)
  better: $P \approx f_{\text{stress}} * E_{\text{tot}} * 1.1$; + 10 % for PCB/stimuli parasitic C)



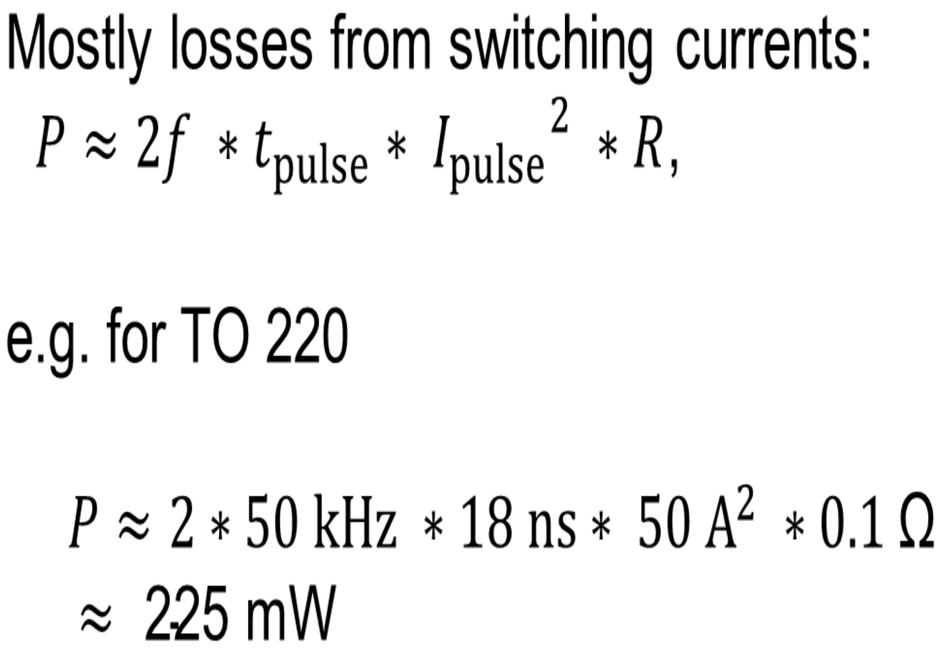
DUT active



Implementing Dynamic H3TRB/DRB

- Possible (non-scientific but helpful) way to estimate rough expectation for DUT passive heating

DUT passive



Mostly losses from switching currents:

$$P \approx 2f * t_{\text{pulse}} * I_{\text{pulse}}{}^2 * R,$$

e.g. for TO 220

$$P \approx 2 * 50\ \text{kHz} * 18\ \text{ns} * 50\ \text{A}^2 * 0.1\ \Omega$$
$$\approx 225\ \text{mW}$$

Mostly losses from switching currents:

$$P \approx 2f * t_{\text{pulse}} * I_{\text{pulse}}{}^2 * R,$$

e.g. for TO 220

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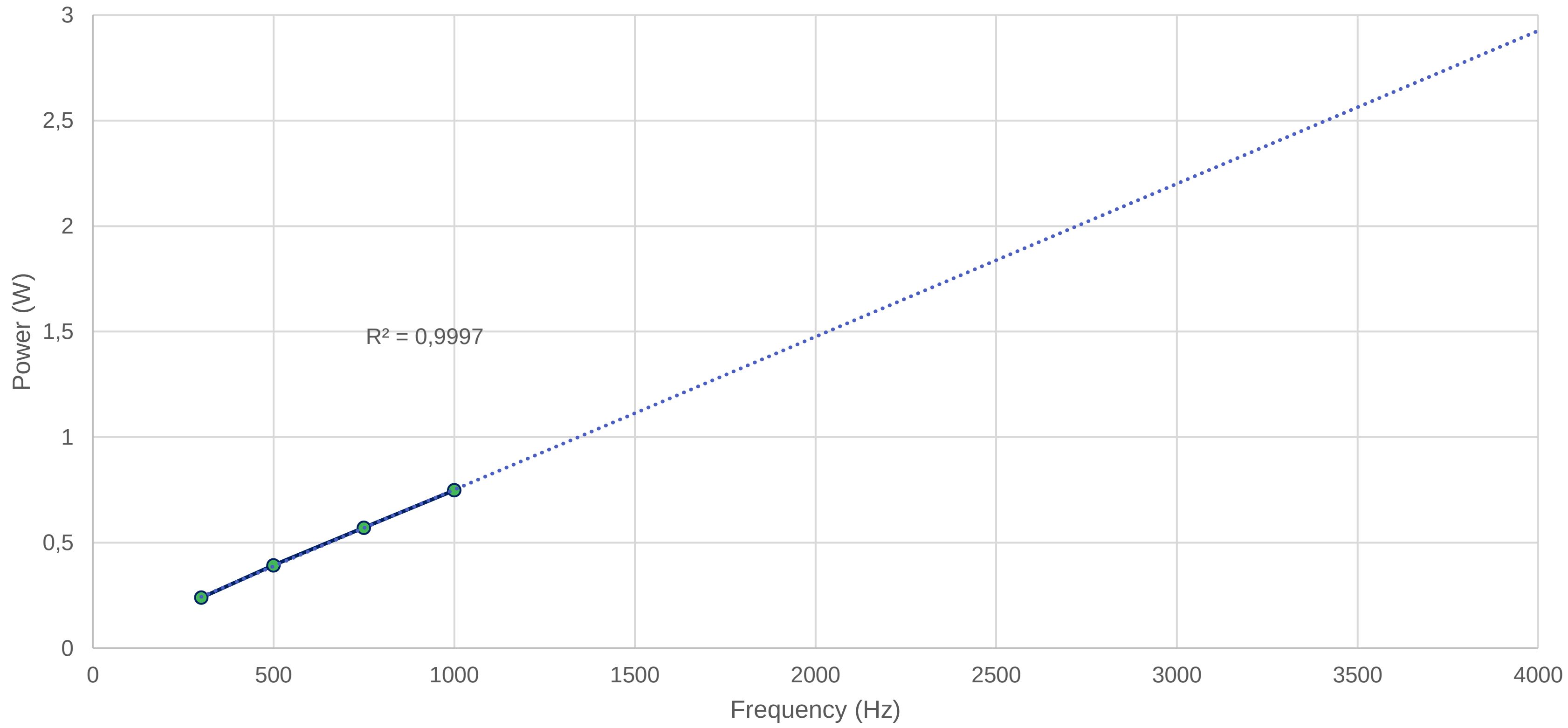
$$\approx 225\ \text{mW}$$

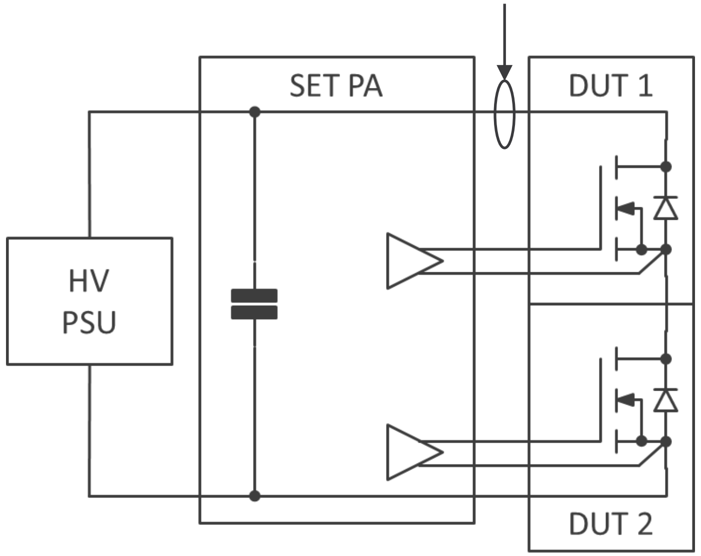
Dynamic H3TRB/DRB in reallife

- even better: measure switching current at low frequency, calculate $P_{\mathrm{DUT}} = I_{\mathrm{sw}} * V_{\mathrm{stress}} * \frac{1}{2}$; $[/2\ \mathrm{DUTs}]$, and scale frequency


Power/DUT

DUT active

Switching current I_{sw}

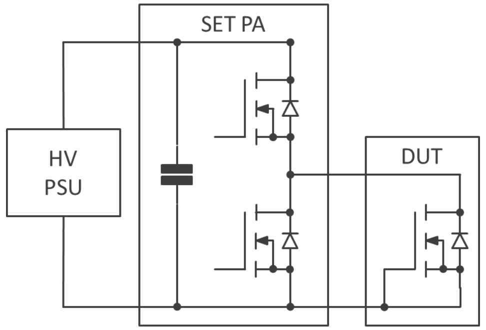


In a nutshell – Dynamic H3TRB/DRB

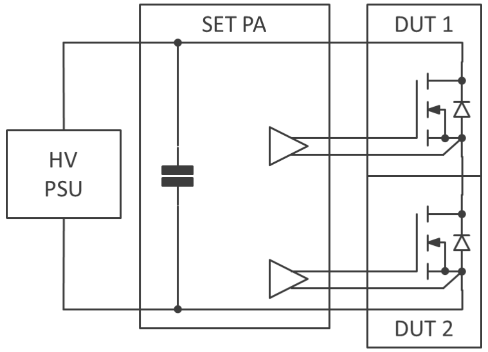
Suggested test parameters

Parameter	Value	Remark
Test duration	≥ 1000 h	
Test ambient	Dyn. H3TRB: 85 °C / 85 % relative humitidy DRB: 25°C	
Stress voltage	Dyn H3TRB: $V_{DS} > 0.5 \times V_{DS,max}$ DRB: $V_{DS} > 0.8 \times V_{DS,max}$ Overshoot: 0.8 to $0.95 \times V_{DS,max}$ dV_{DS}/dt: 30 V/ns to 110 V/ns	Waveform matters! Use of 0.2/0.8 can be considered
Stress frequency	DUT active: 5 kHz to 25 kHz DUT passive: 15 kHz to 400 kHz	Mostly depended on power in DUT
Gate voltage	$V_{GS,off}$: $V_{GS,min.recom}$ $V_{GS,on}$: $V_{GS,max}$	Avoid PTO and undershoots!

DUT passive



DUT active



Measurement	Readout time	Remark
$I_{DS,leak}$	begin, end (minimum) all 5 min (recommended)	Can show degradation before breakdown

NI Reliability offering

Systems to test for new Effects

NI/SET – Power Reliability Turn-key Solutions

General:

- Highly automated test sequencing, freely configurable
- COTS speed up lead times and maintenance
- Scalable whilst project or after delivery extension
- Standardized DUT-connection interfaces, minimizing custom adaptation efforts connecting a variety of DUT types, for example:
  - discrete packages
  - half-bridge, power modules
  - B6-bridge, inverters

Solutions according to lifetime testing guidelines:

- AQG-324: QL-01, QL-02
- AQG-324: QL-05, QL-06, QL-07
- AQG-324: QL-06a
- AQG-324: QL-05a, QL-07a
- AEC-Q101: #10

Released

Dynamic H3TRB/DRB AC-HTC 2.0

- **Primary Application Targets:**
- Power electronics qualification
- AQG 324 conform DRB & dyn H3TRB test
- Automotive / Renewable Energy Mission Profiles

- **Key Features:**
- Up to 240 DUTs
- Supports DUT active & DUT passive
- Up to 1500V stimuli, suitable for up to 1.7kV V_{ds}
- Typical dV/dt 30-100V/ns, up 350 kHz in DUT passive

- **Roadmap Feature:**
- AC-HTC 2.0 stress profiles (Q3/24)

Dyn H3TRB / DRB
Roadmap: AC-HTC 2.0

Released

Dynamic Gate Stress (DGS)

- **Primary Application Targets:**
  - Power electronics qualification
  - Gate Oxide instability test
  - AQG 324 QL-06a conform test

- **Key Features:**
  - Up to 240 DUTs in a 19” rack
  - JEDEC JEP 183 compliant Vth in-situ readout
  - Software configurable V_{gs} = ± 30V max
  - High dv/dt stimuli at up to 300kHz
  - Hot/cold plate ranging from 20°C to 200°C

DGS / dyn HTGB

Testing as a Service

- Extensive engineering support for test setup and execution
- Application / nonstandard tests on request
- Detailed test reports
- DUT adaption service

Standard tests provided:

Power cycling:	AQG-324: QL-01, QL-02
HTRB:	AQG-324: QL-05,
DRB:	AQG-324: QL-05a
HTGB:	AQG-324: QL-06
DGS:	AQG-324: QL-06a
H3TRB:	AQG-324: QL-07
Dyn. H3TRB:	AQG-324: QL-07a
IOL:	AEC-Q101

EMERSON | NI

Thank you!!

Questions??

CONNECT

NI is now part of Emerson.

CONNECT

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