

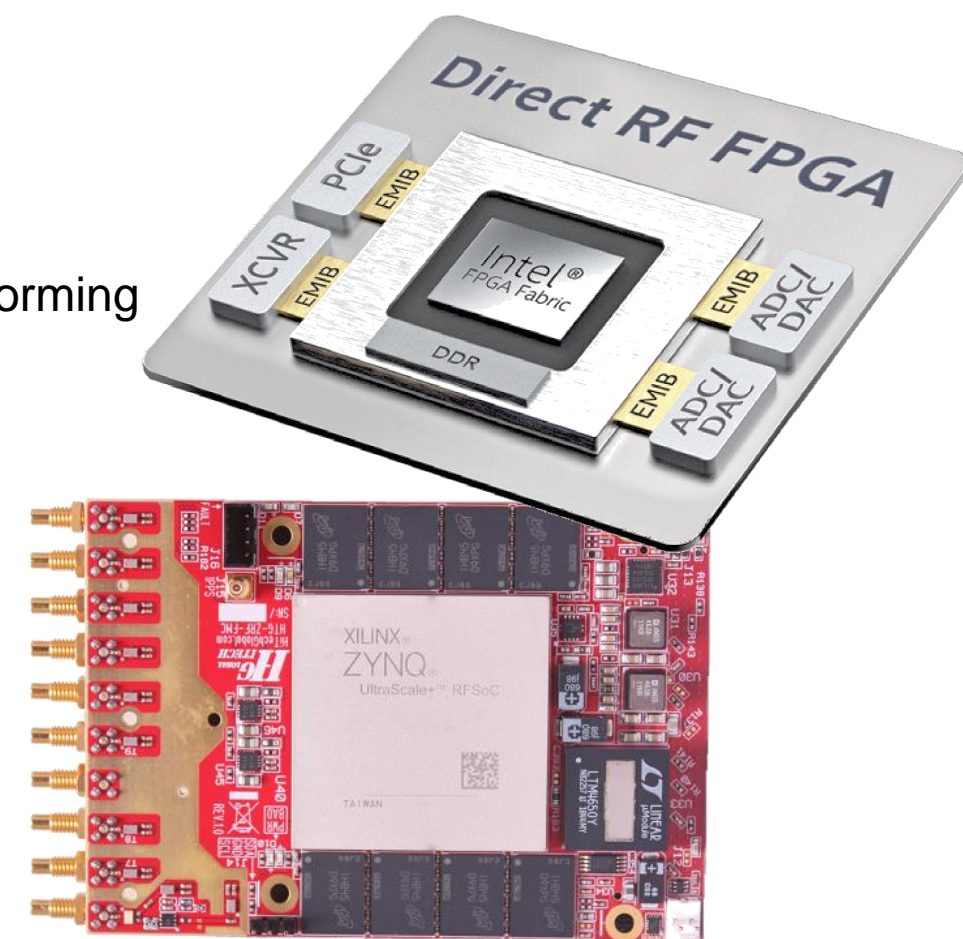
# **‘Direct RF to Bits’ Testing**

Introducing the Digital Signal Transceiver (DST)

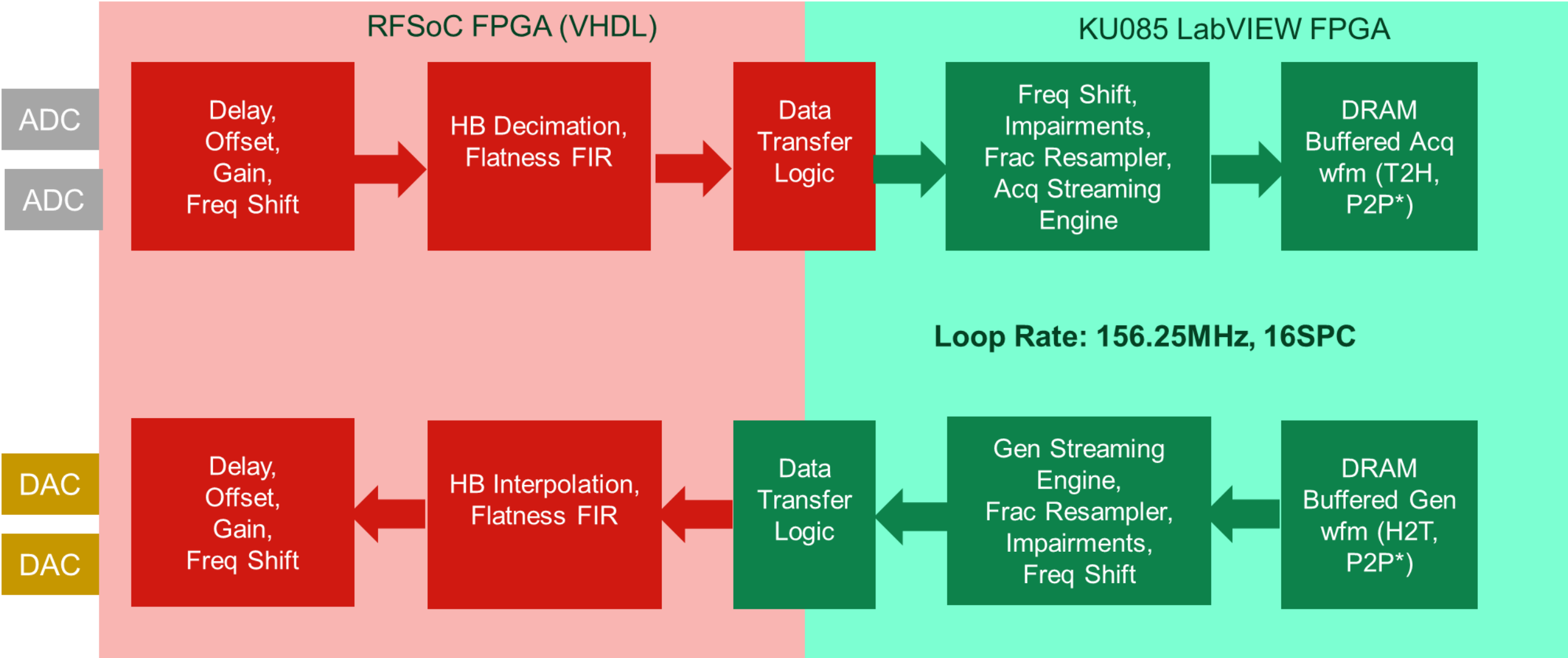
# Define 'RF to Bits' Devices

## RFSoc Enabled Devices Capable of Direct Sampling Wide-Band RF Signals

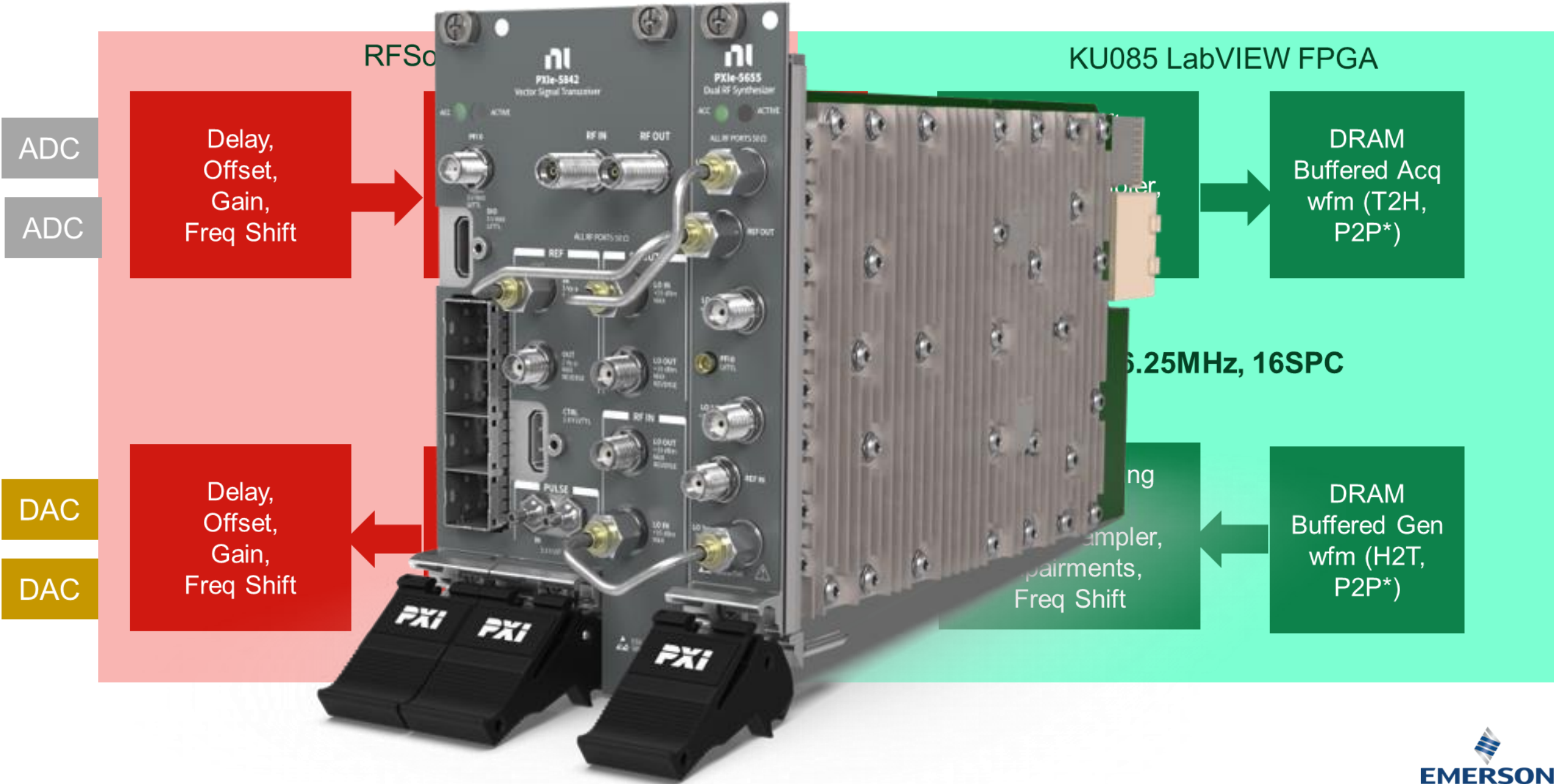
- Commonly sampling above 6GSa/sec to rates >64GSa/sec
- Significantly decreases component count to perform common operations like beamforming
- Digitally up/down converts signals and performs basic processing (gain, phase, eq)
- Requires digital bandwidths up to and beyond 100Gb/sec
- Flexible onboard FPGA with MGT streams to secondary processor
- Breaks common RF paradigm for using a VNA to test everything



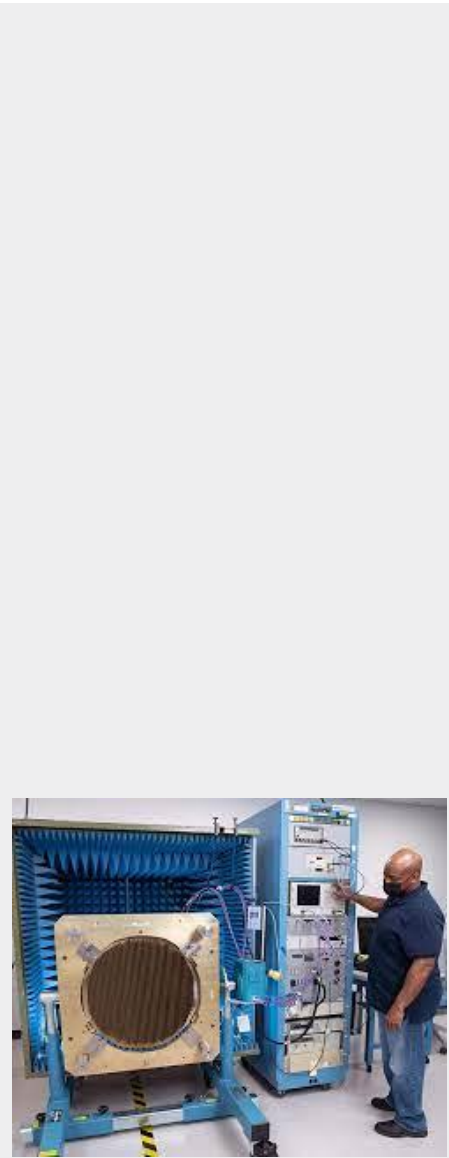
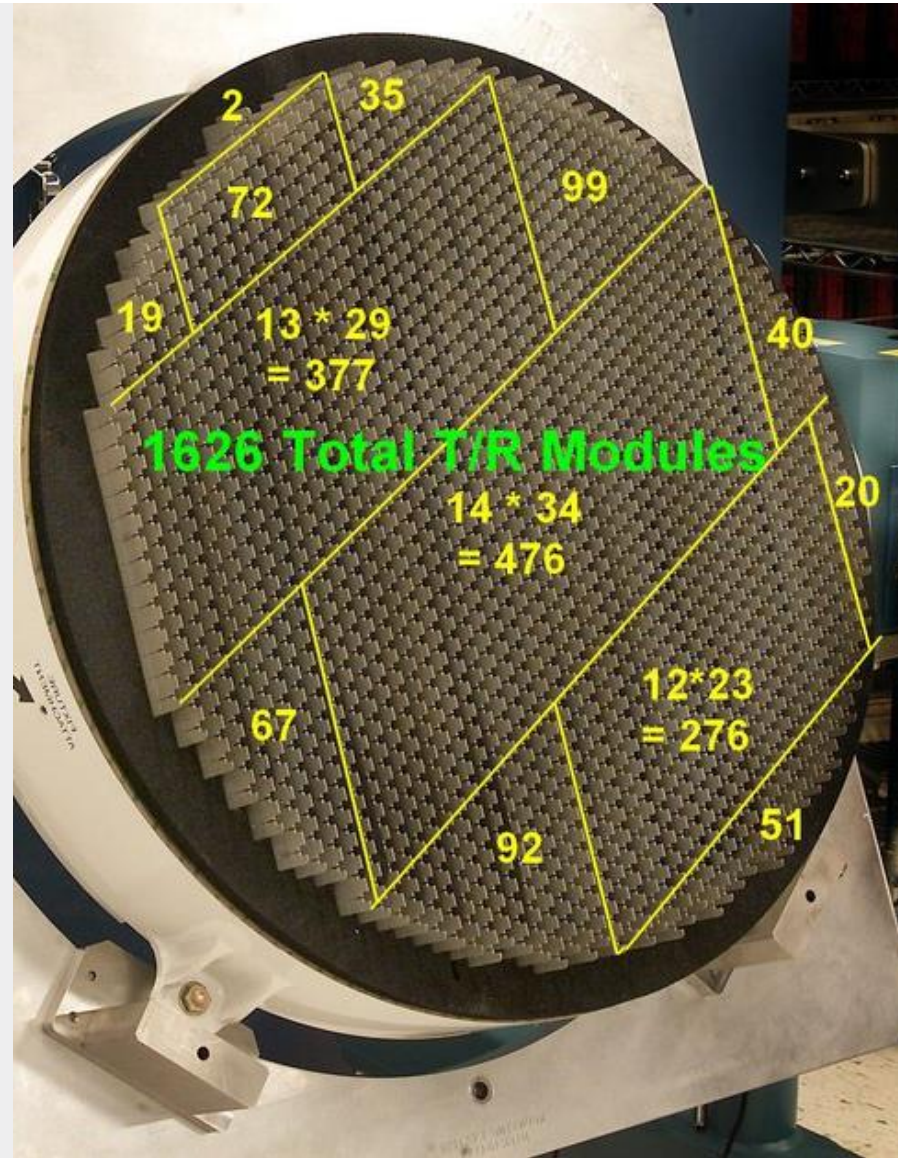
# PXle-5842 VST – 5GSa/s ‘RFSoc’ Device



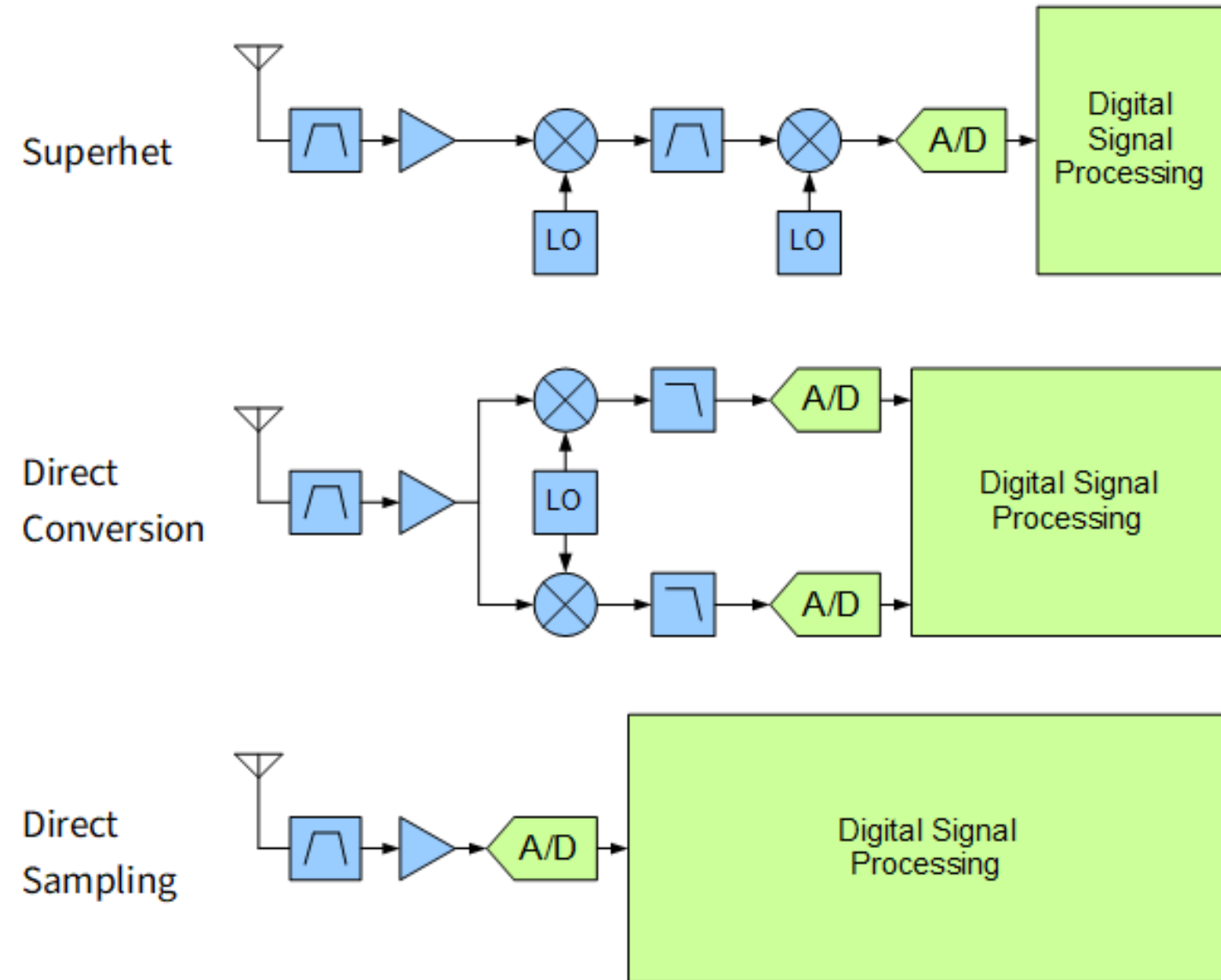
# PXIe-5842 VST – 5GSa/s ‘RFSoc’ Device



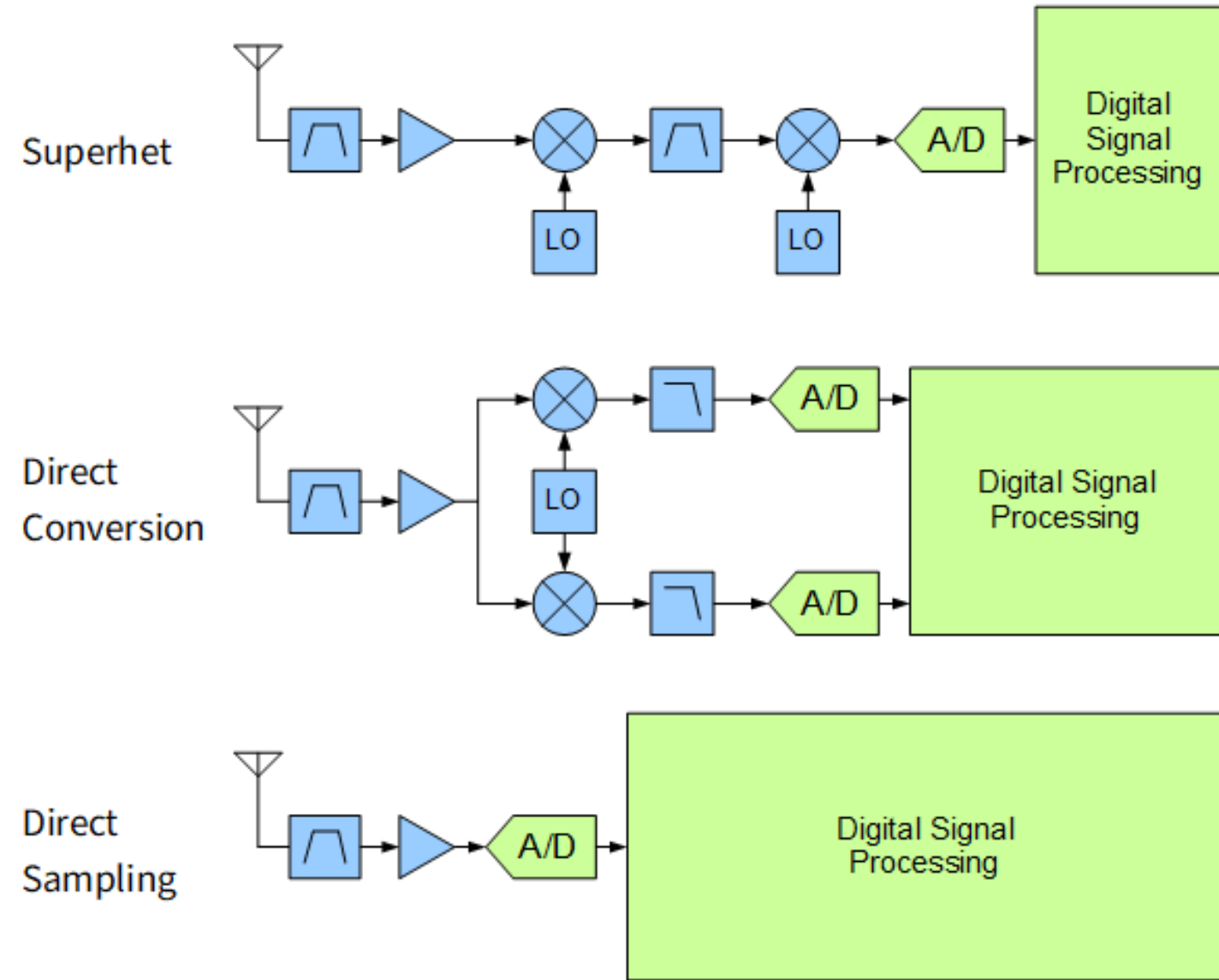
# Application: 'RF to Bits' Transmit Receive Systems



Human for Scale

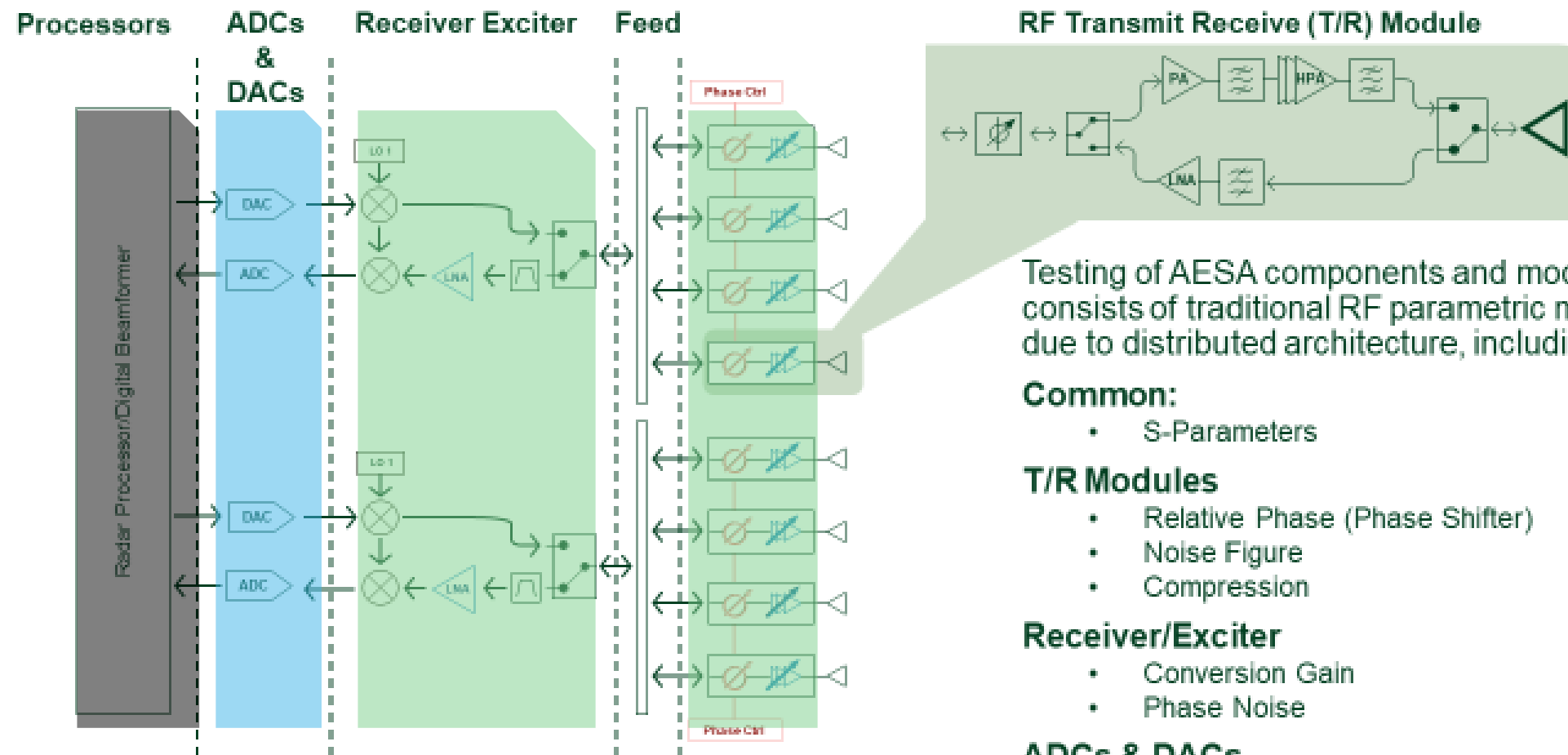


# Application: 'RF to Bits' Transmit Receive Systems



# Industry Situation

Active Electronically Scanned Array (AESA) antenna systems & signal chains have evolved from multiple, discretely testable, analog modules into digitally dominated transceiver systems with directly integrated high speed converters (ADC/DAC).



Historical Test Boundaries Maintained – RF components and modules, Low frequency Data Converters, and Digital Processors

Testing of AESA components and modules largely consists of traditional RF parametric measurements due to distributed architecture, including:

**Common:**

- S-Parameters

**T/R Modules**

- Relative Phase (Phase Shifter)
- Noise Figure
- Compression

**Receiver/Exciter**

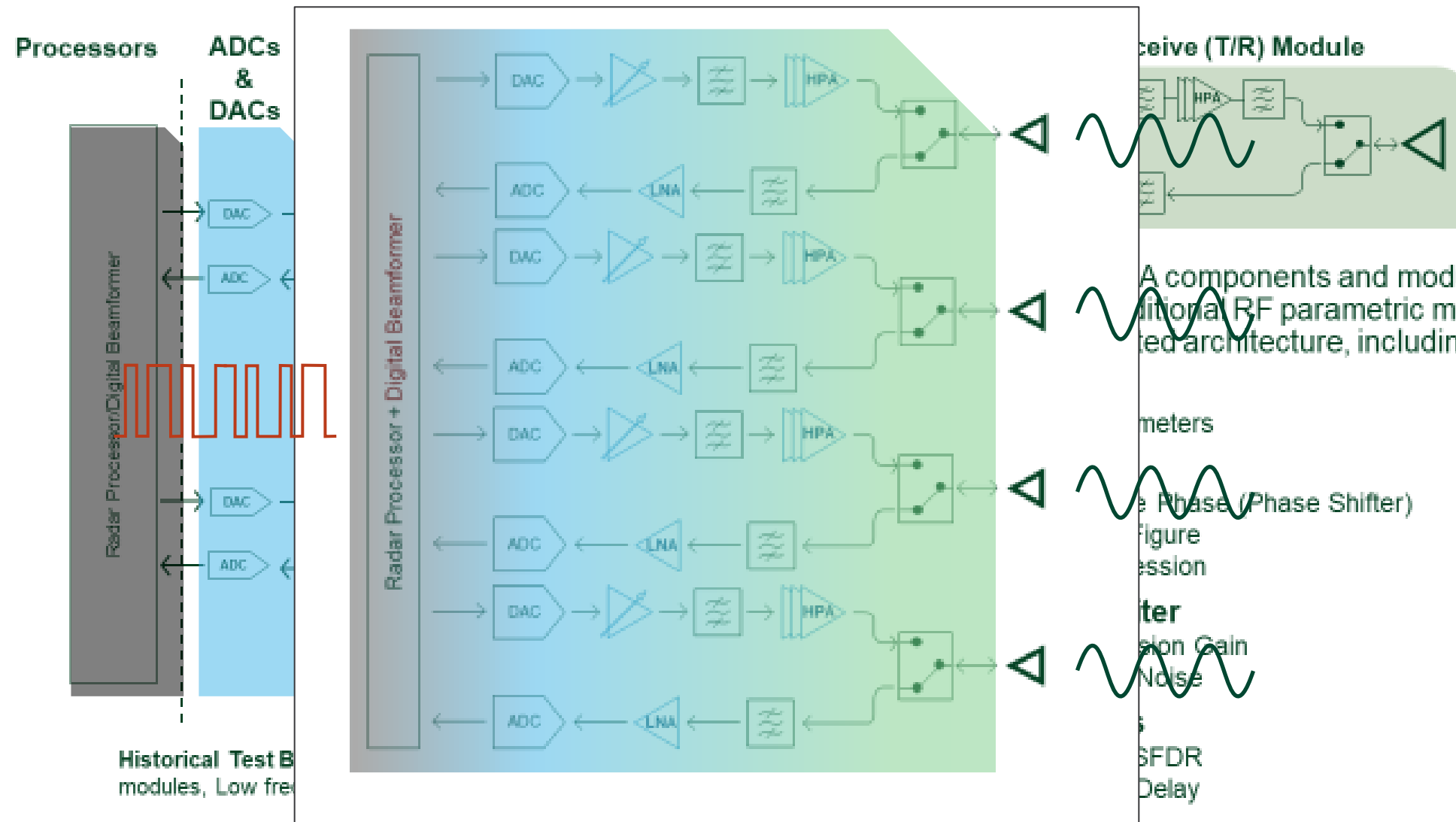
- Conversion Gain
- Phase Noise

**ADCs & DACs**

- SNR / SFDR
- Group Delay

# Industry Situation

Active Electronically Scanned Array (AESA) antenna systems & signal chains have evolved from multiple, discretely testable, analog modules into digitally dominated transceiver systems with directly integrated high speed converters (ADC/DAC).



A components and modules largely  
 additional RF parametric measurements  
 ed architecture, including:

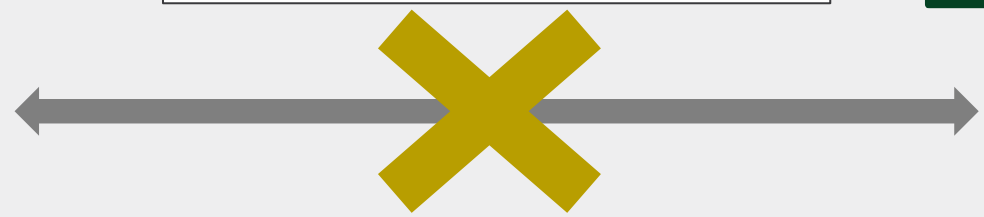
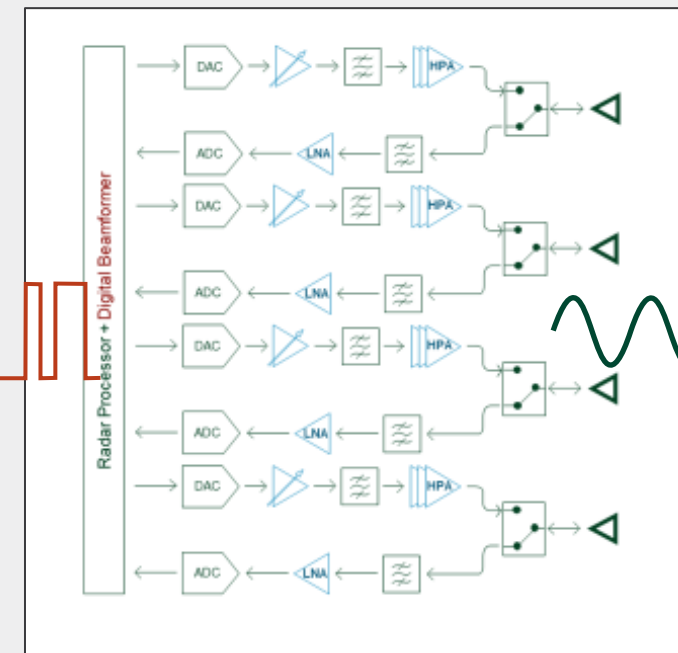
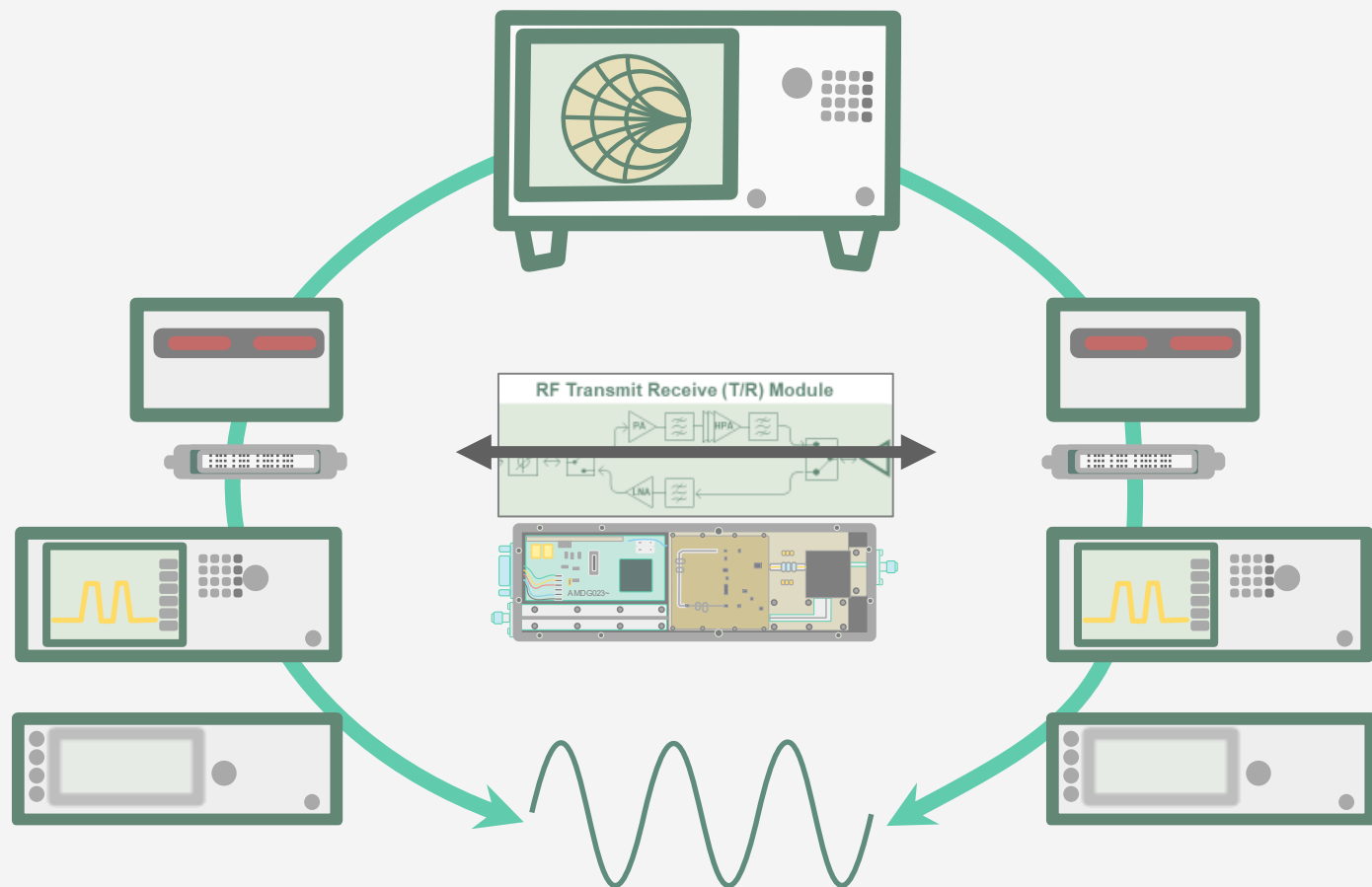
- imeters
- Phase (Phase Shifter)
- Figure
- ession
- ter
- ation Gain
- Noise
- SFDR
- Delay





# Industry Challenge

Traditional AESA measurement methodologies and instruments, commonly utilizing analog VNAs, are incapable of fully addressing the modern signal & demands of these newly digitally integrated transceiver modules (DTRM).

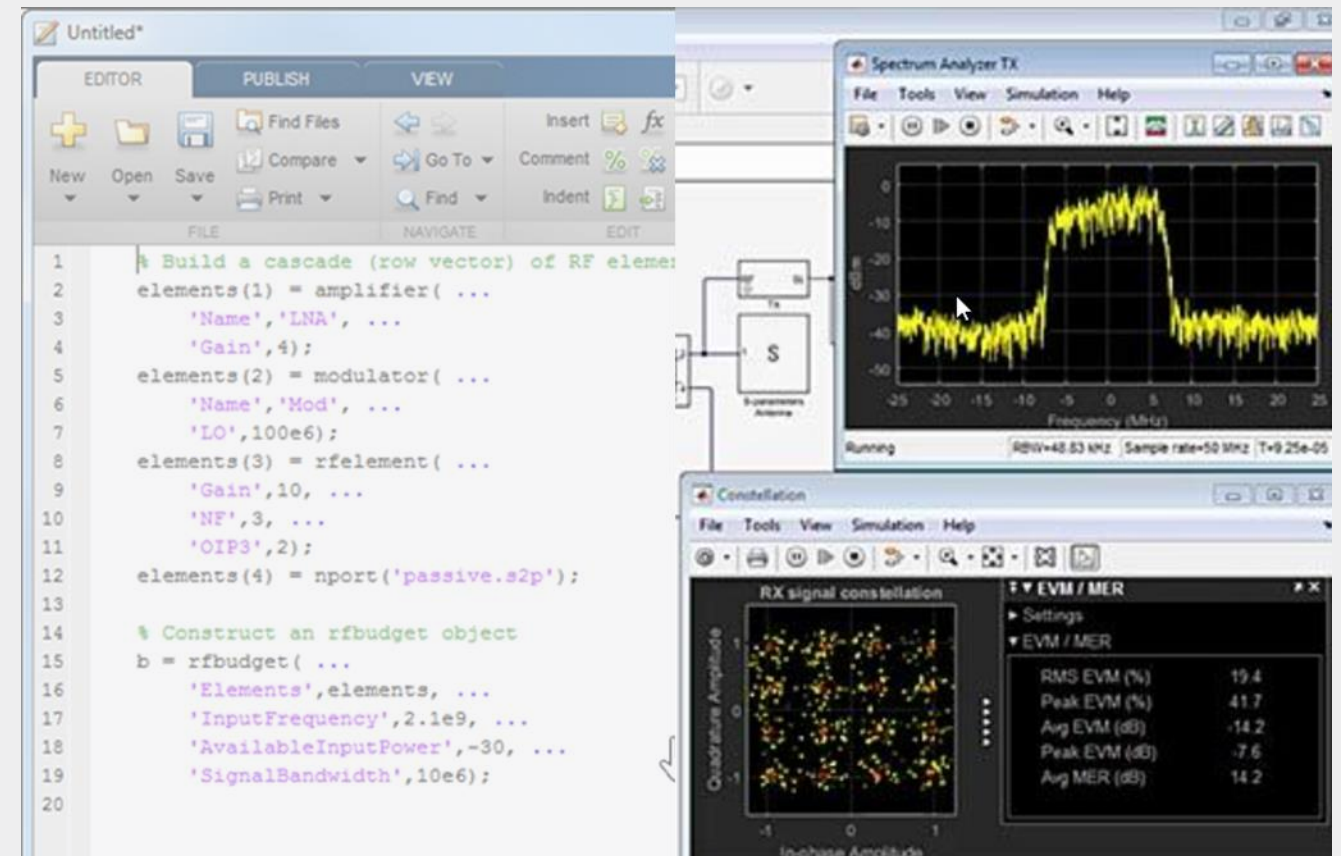


# Problem Breakdown

Digital Connectivity Not Ready To Scale



Underperforming Measurement Science



# What Connects to Your Digital?

## Evaluation / Home-Grown 'Solutions'

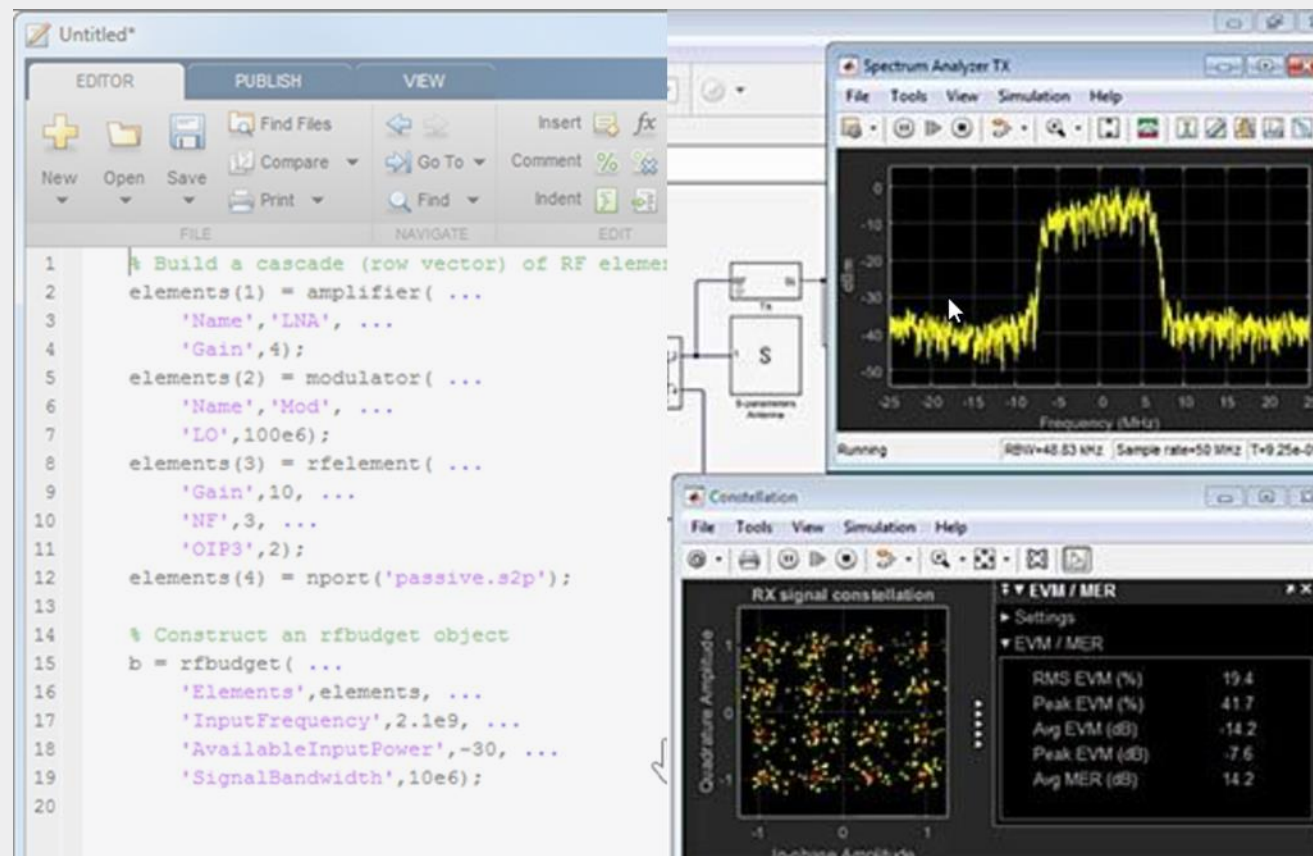
- Test departments not equipped with High-Speed-Serial (HSS) interfaces
- Home-grown digital solutions costly and difficult to produce at scale, maintain and deploy over a program's lifecycle
- Evaluation boards not designed or manufactured to be long term scalable solutions
- Memory and data transfer size and rates limit test time performance
- Not suited for production or your SUT connectivity demands

## Functional but Not Practical at Production



# How Do You Calibrate and Correlate?

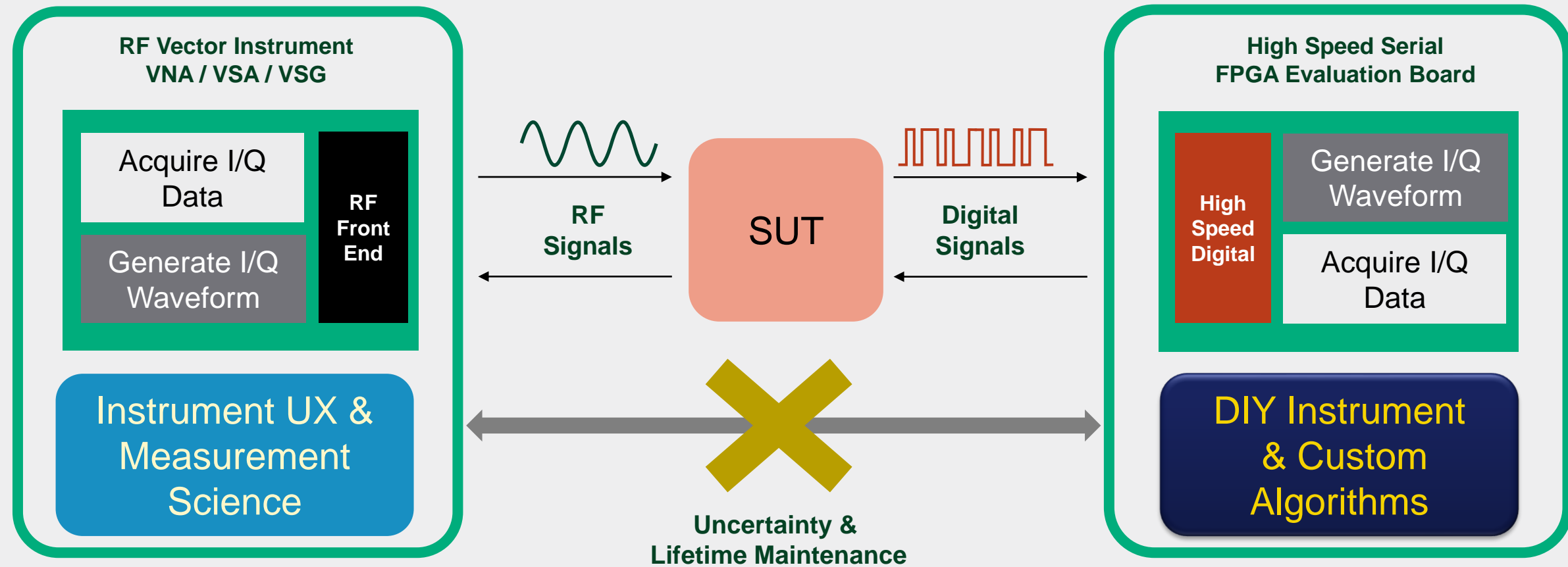
## Slow Results on Custom Algorithms



## Spend time measuring your device and not developing Instrumentation IP

- Moving large data around memory or files is inherently slow
- Developing algorithms that display a result are easy, getting to good results you to correlate is hard
- Stimulus response measurements should have instrumentation on both stimulus and response
- Most custom algorithms and API are not developed for scalability, long term maintenance or speed
- Complex measurements like pulse profile analysis should be common regardless of domain (analog or digital)

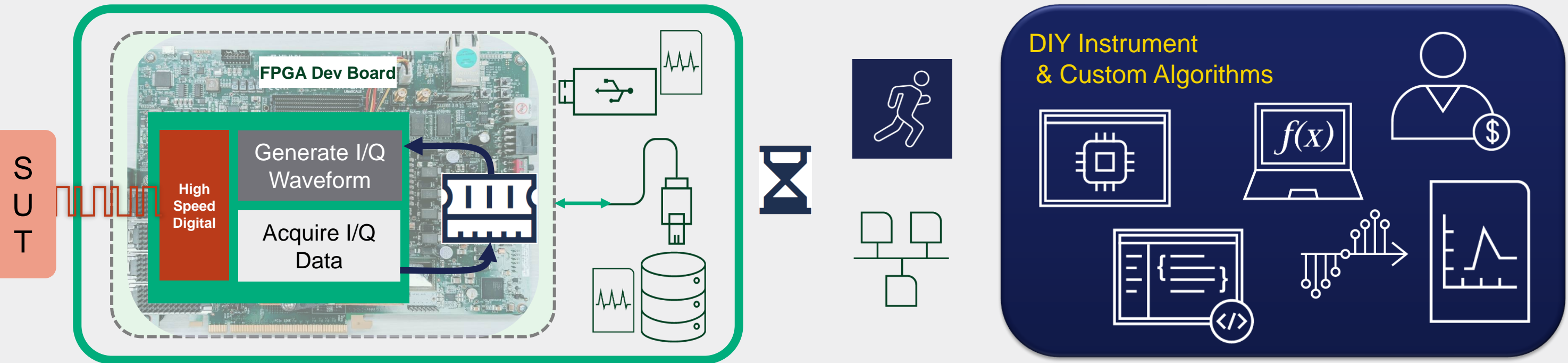
# RF to Digital Workflows



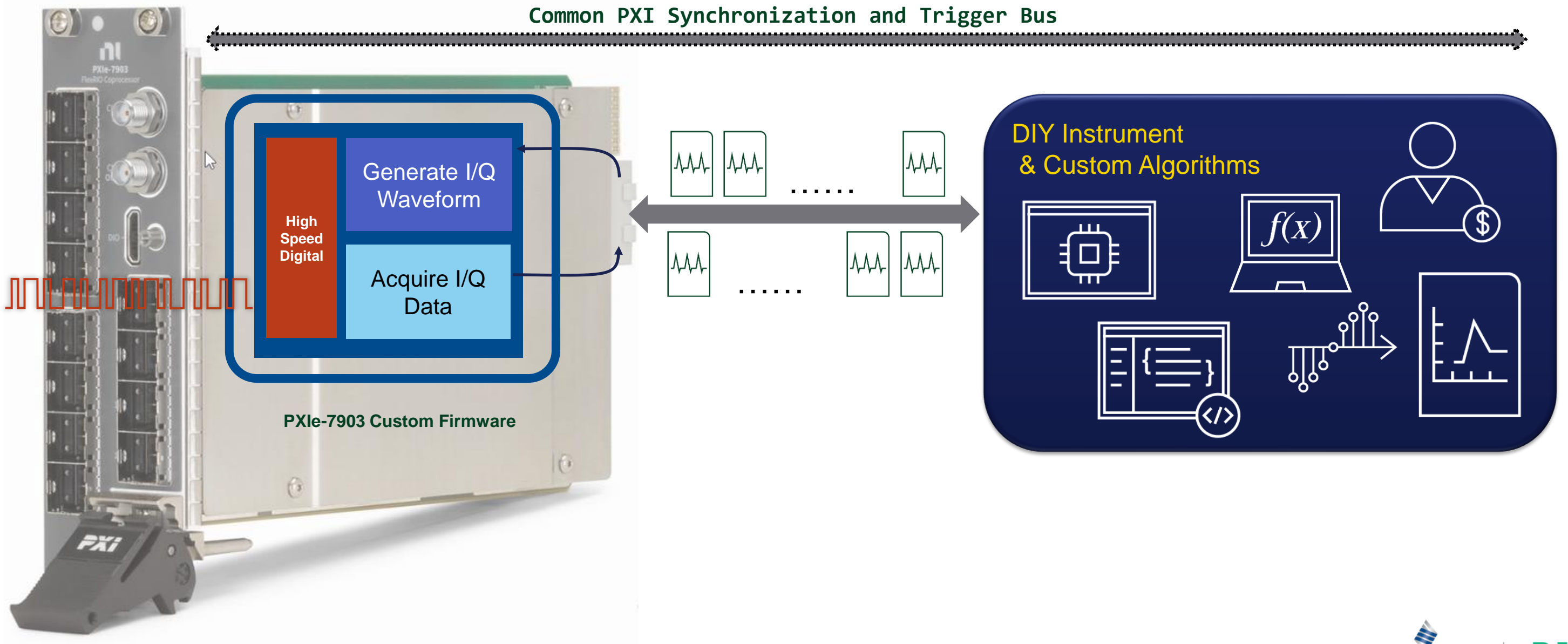


# RF to Digital Workflows

## Save/Load Memory Model

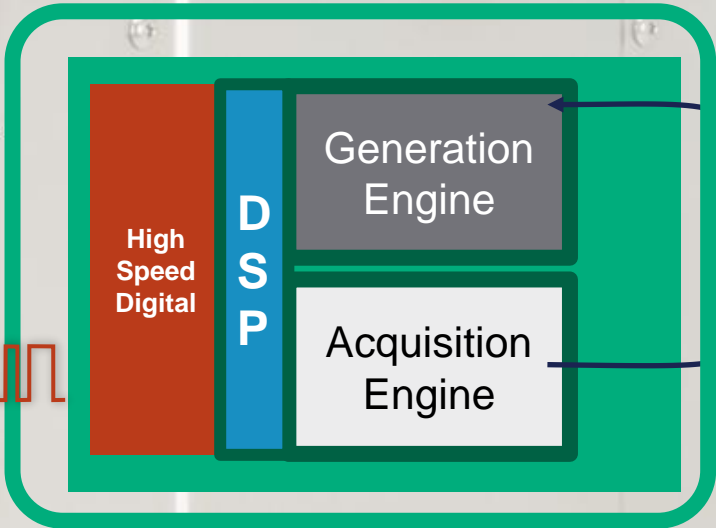


# DIY Digital Instrument Model

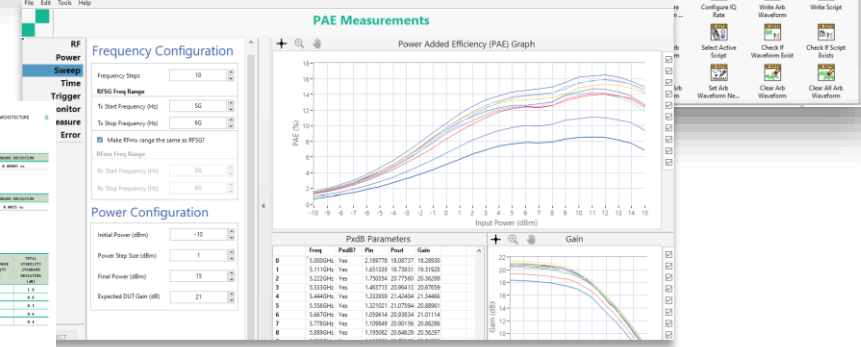
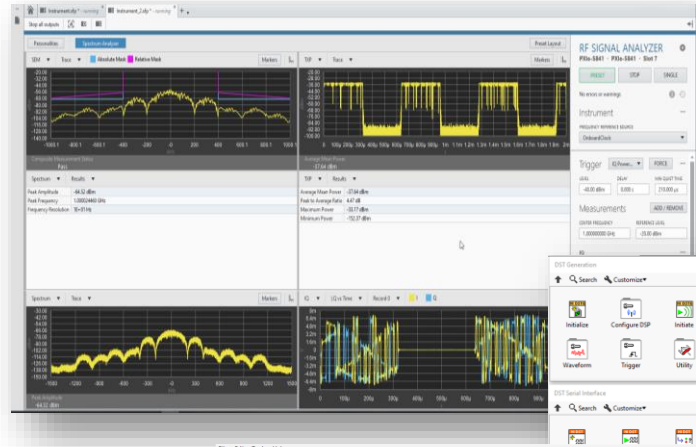
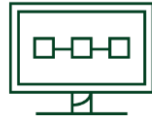
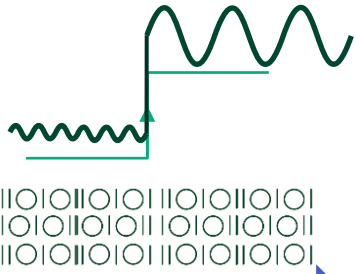


# DST - Digital Signal Transceiver

Common PXI Synchronization and Trigger Bus



PXIe-7903 & DST Image  
+  
Custom Digital Front End



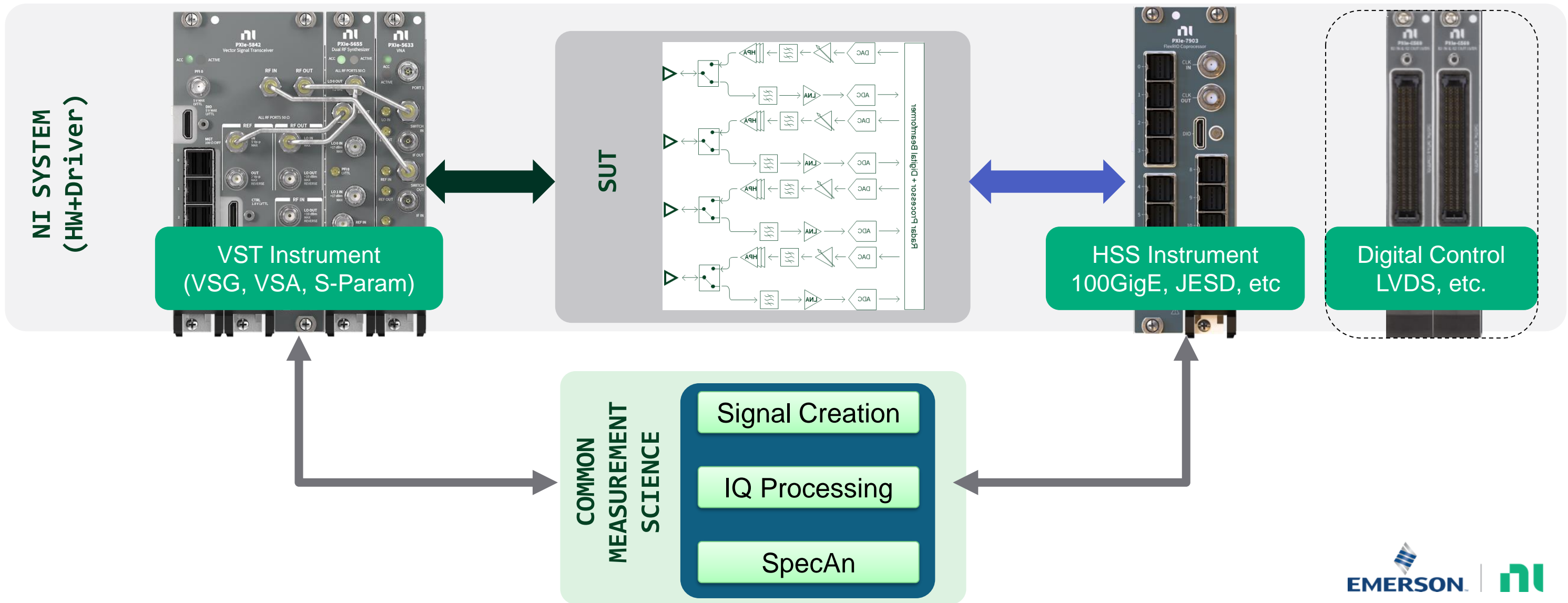
INNER  
PEACE



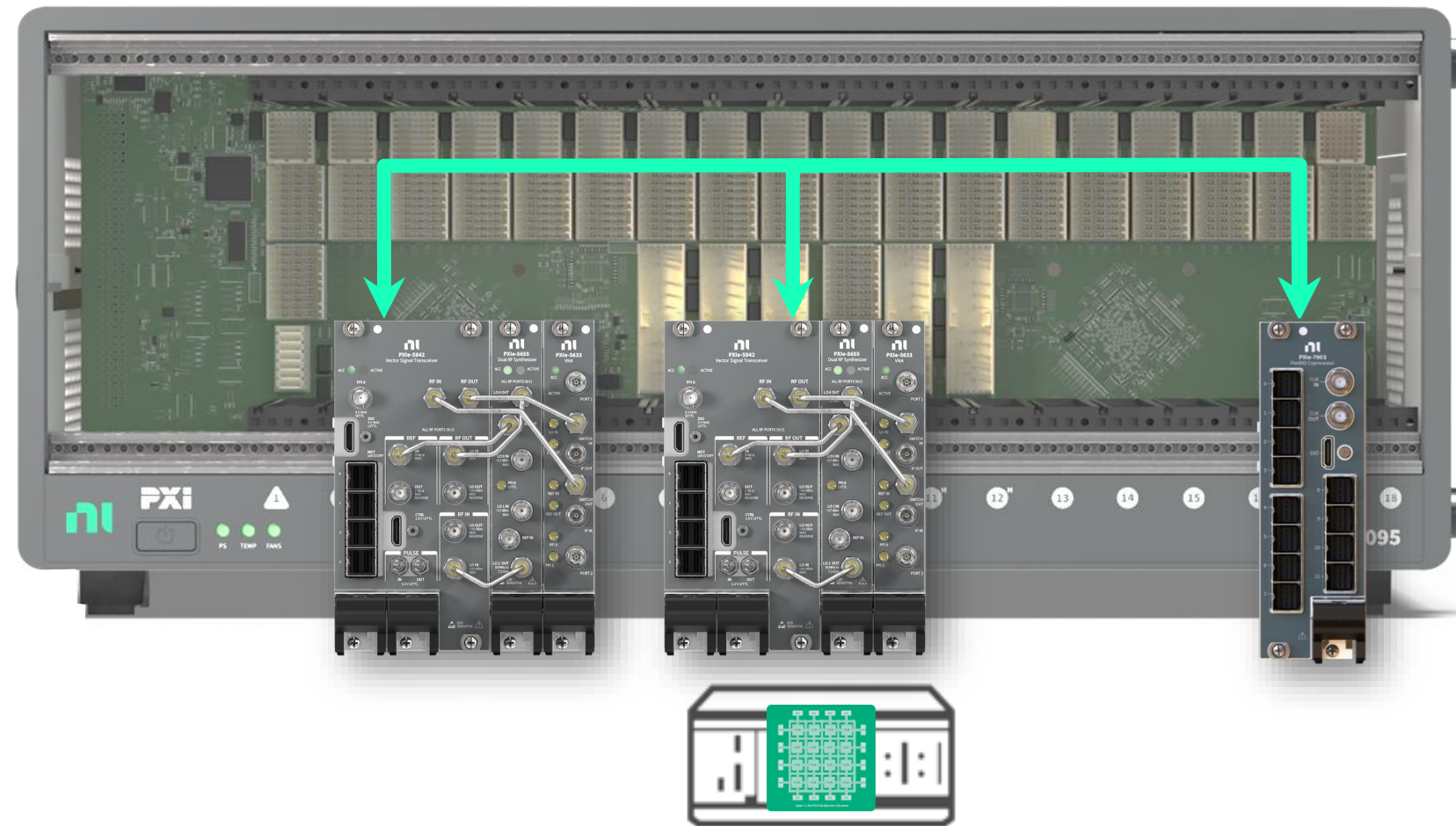
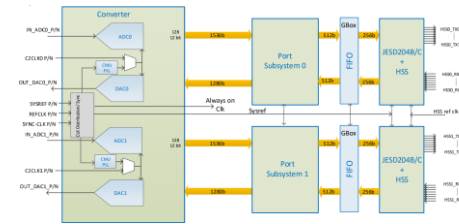


# Re-establishing the Instrumentation Hug

Common PXI Synchronization and Trigger Bus



# Instrument Coordination View



Common PXI Synchronization and Trigger Bus

# System Under Test



# Preview Demo

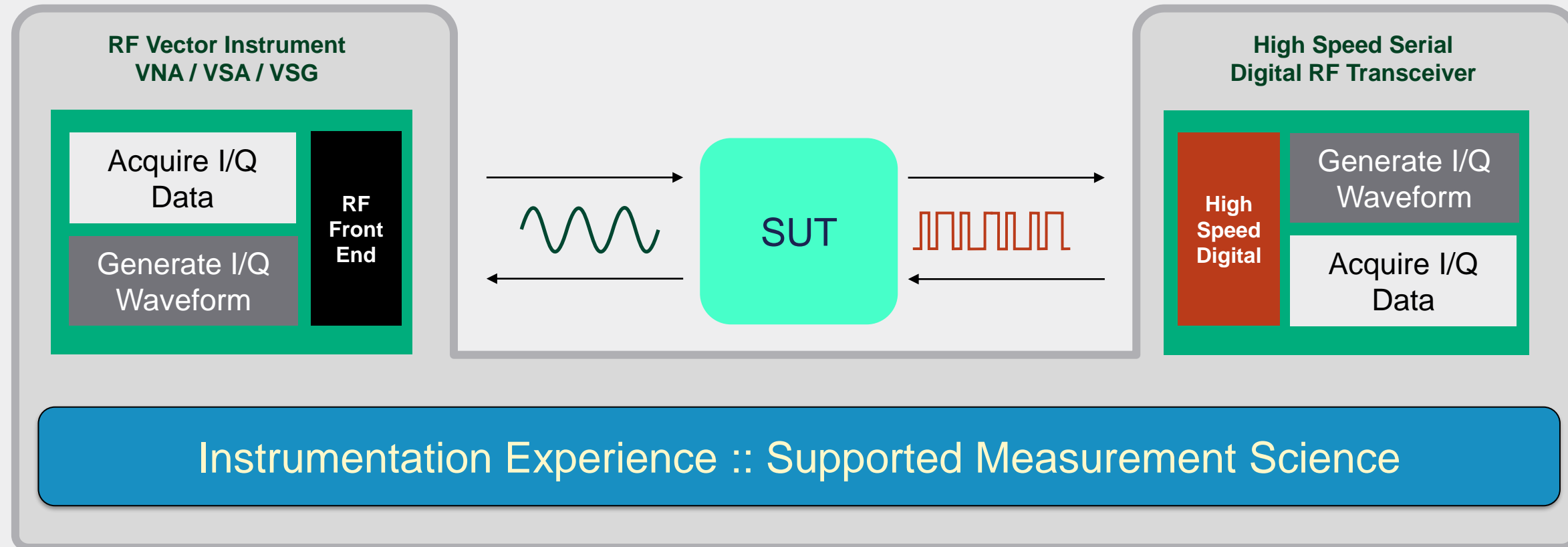
# DST Instrument Workflow

## Design and Development Accelerators

- **Interactive** out of the box
  - No-code acquisition and visualization
  - Debug platform for designers
  - Extensible interface through Instrument Studio
- Instrument Grade **Automation API**
  - Features and interfaces mirrored from RFSA/G
  - Powerful trigger engines
  - Waveform scripting
  - Stream data or capture records

# RF to Digital Workflows

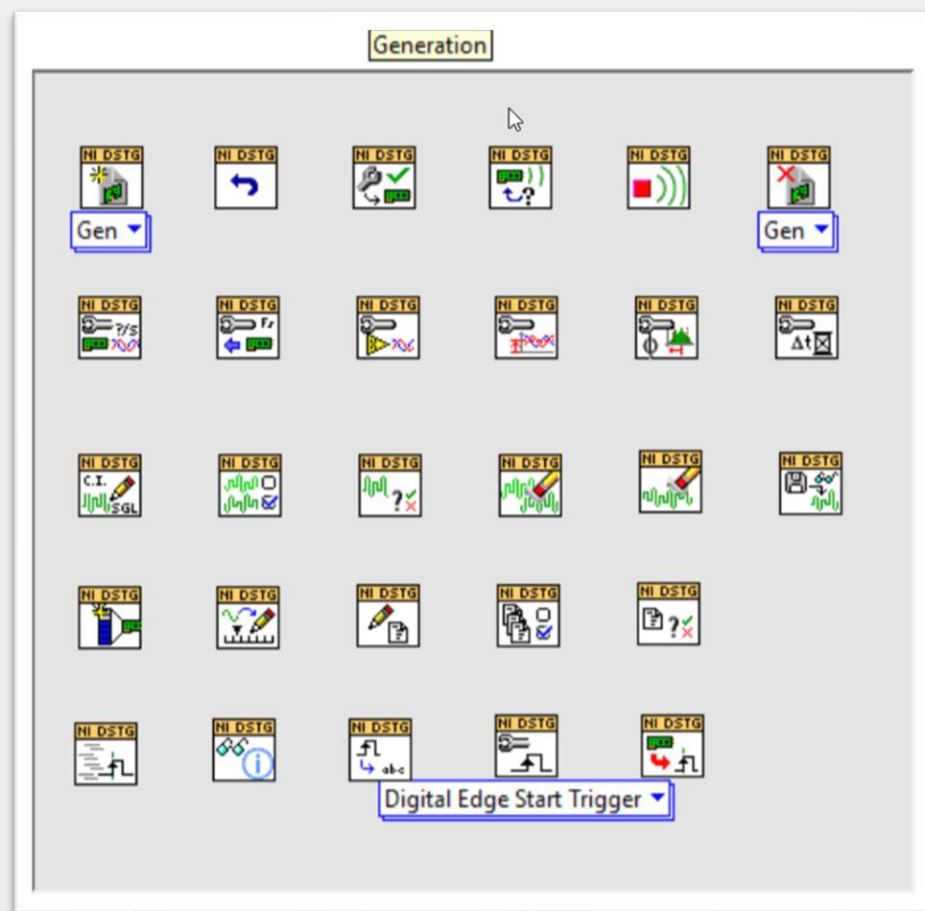
## Digital RF Vector Instrument Model



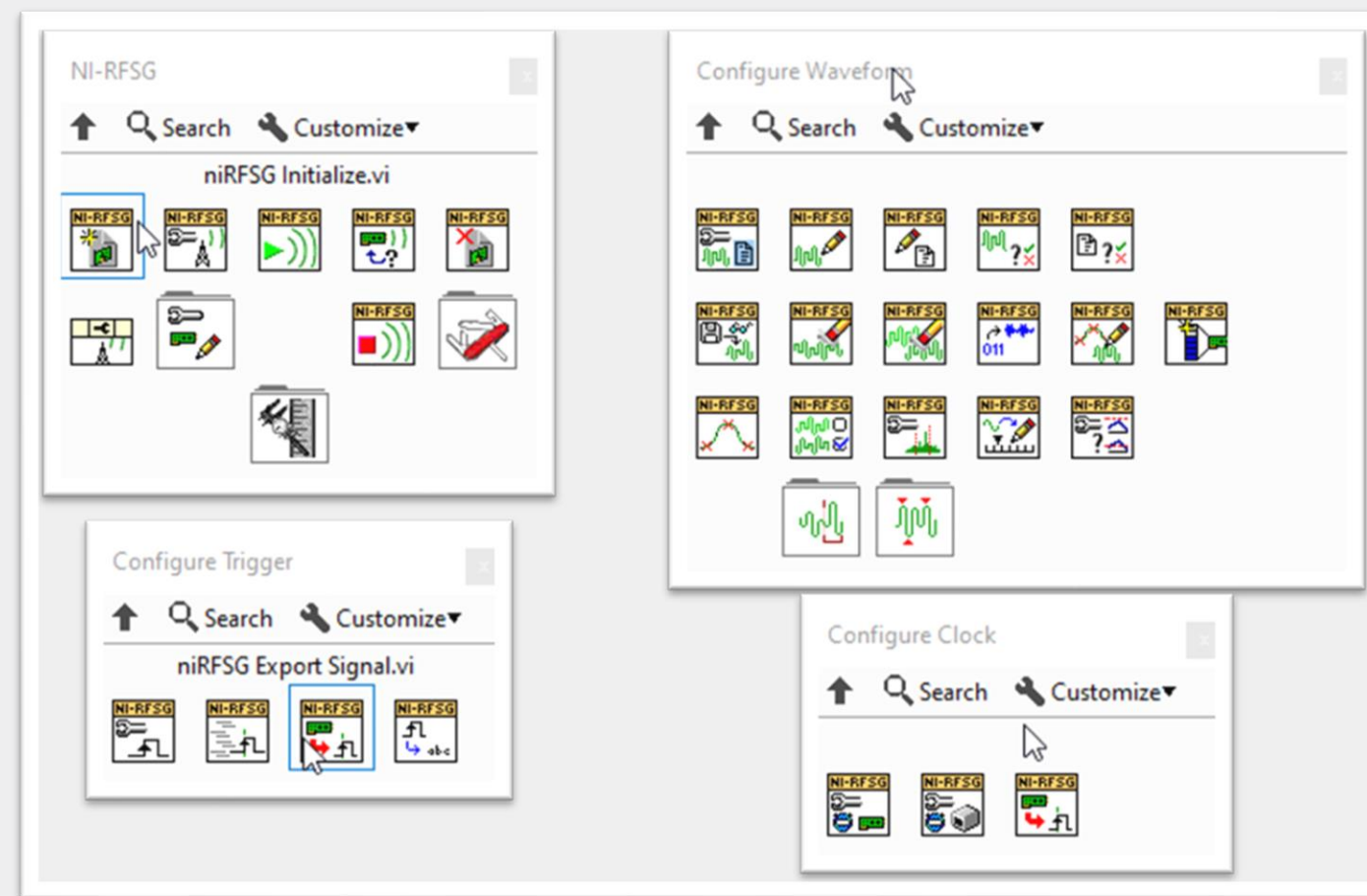
**Desired Instrumentation – I/Q Stimulus and Response**

# Instrument Grade API – Generation Comparison

## DST-G



## NI-RFSG



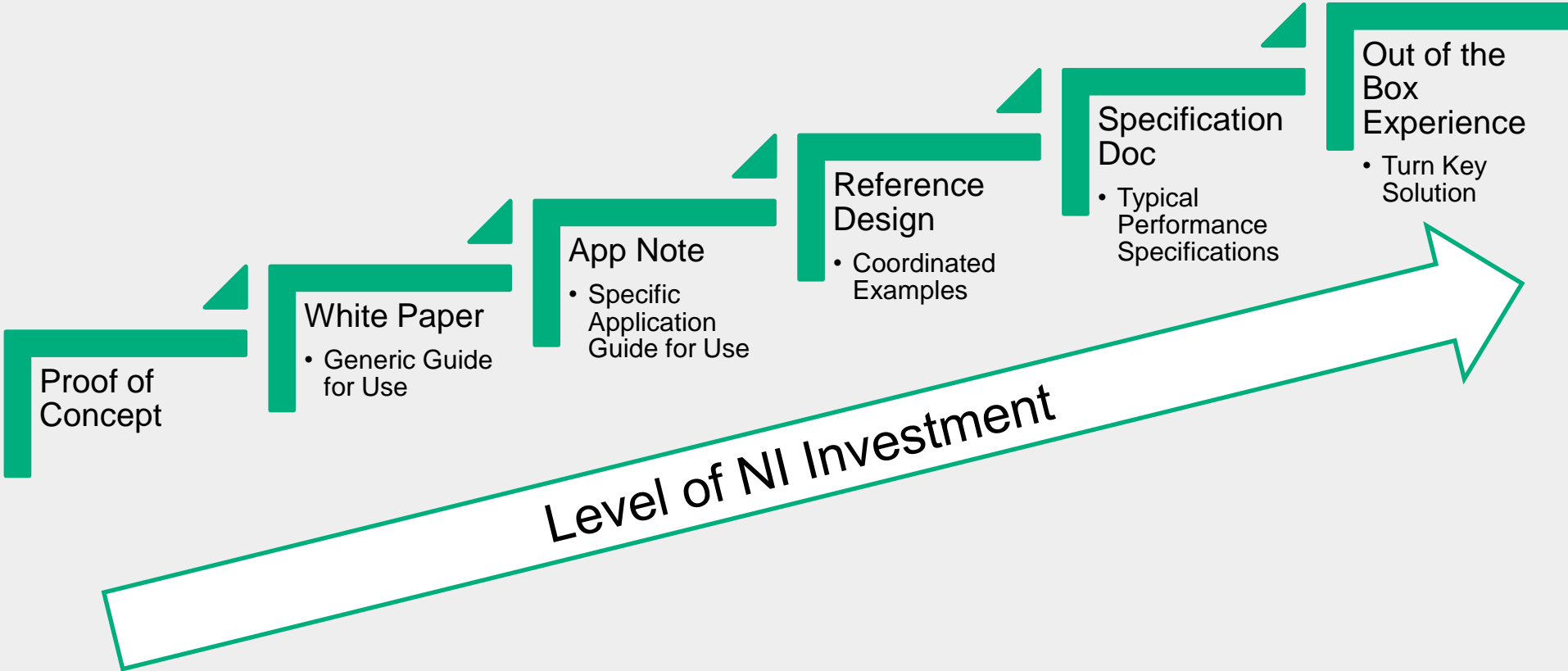
# Full Pallet Overview

The image displays a collection of software interface panels, each containing a grid of icons for different functions. The panels are organized into several groups:

- DST Generation:** Includes panels for 'DST Generation' (top left and middle left) and 'DST Acquisition' (top right). Functions include Initialize, Configure DSP, Initiate, Abort, Close, Waveform, Trigger, Utility, and Check Gen Status. The 'DST Acquisition' panel also includes IQ and Fetch IQ.
- DST Serial Interface:** A panel (middle left) with functions like Initialize, Initiate, Get Status, Abort, Close, Configure Parameter, Get Parameter, Write, Read, Reset, Get Serial Interface, and Set Serial Interface.
- Configure Waveform:** A panel (middle) with functions such as Configure Generation..., Configure IQ Rate, Write Arb Waveform, Write Script, Select Arb Waveform, Select Active Script, Check If Waveform Exist, Check If Script Exists, Allocate Arb Waveform, Set Arb Waveform Ne..., Clear Arb Waveform, and Clear All Arb Waveform.
- Configure DSP:** A panel (middle right) with functions like Configure Digital Gain, Configure Digital Offset, Configure Dig Freq Shift, Configure Ref Trigger Delay, and Configure IQ Rate.
- Configure DSP (Bottom Left):** A panel with functions like Configure Digital Gain, Configure Digital Offset, Configure Dig Freq Shift, Configure Gen Delay, Configure IQ Rate, and Configure Gen Sample Rate.
- Trigger:** A panel (bottom middle) with functions like Configure Trigger, Send Software Trigger Edge, Export Signal, and Get Terminal Name.
- Utility:** A panel (bottom middle) with functions like Commit, Reset, Get Configuration, and Get Information.
- IQ:** A panel (bottom right) with functions like Configure Acq Sample Rate, Configure IQ Rate, Configure Num Samples, and Configure Num Records.
- Trigger (Bottom Right):** A panel with functions like Configure Trigger, Send Software Edge Trigger, Export Signal, and Get Terminal Name.
- Utility (Bottom Right):** A panel with functions like Commit, Reset, Get Information, and Get Configuration.

# Easing the Struggle

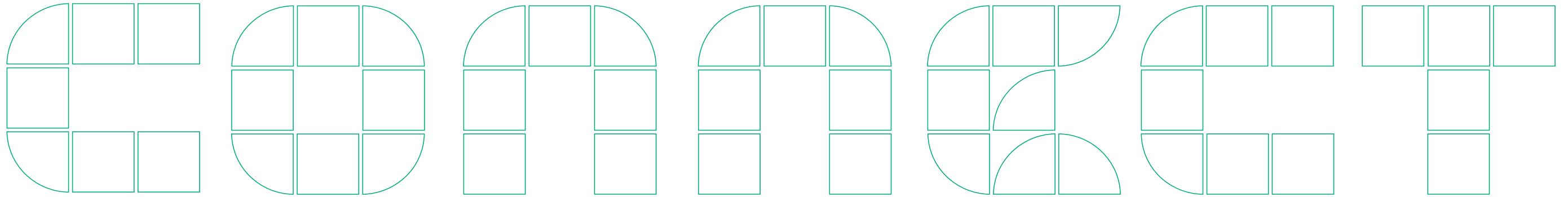
## NI Tiers of Service



## Optimizing Support

- NI is able to provide Levels of Service that meet the needs of each customer
- Identifying the level of investment that is value added for YOU the customer is key to **enabling** and **accelerating** your success





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