APPLICATION NOTE

Setting Up ADC Measurements with NI's Data Converter Reference Architecture

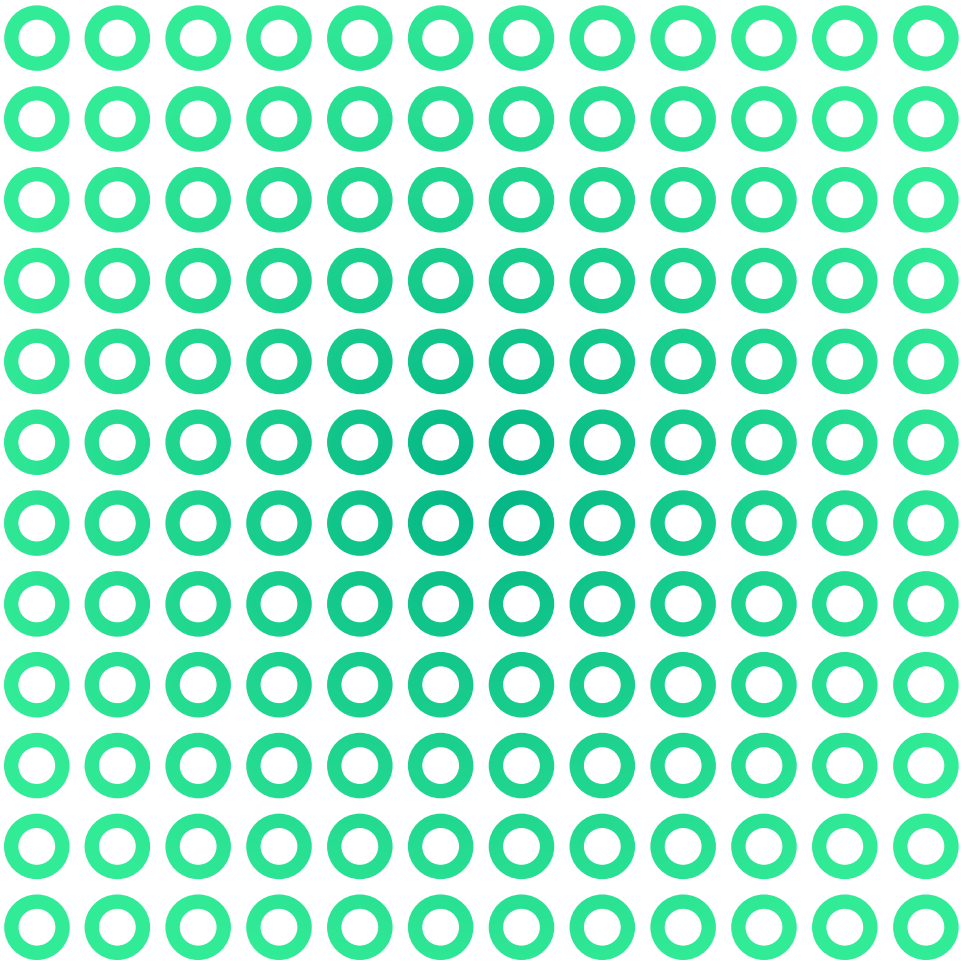

Table of Contents

This application note describes how to set up ADC measurements using NI's Data Converter Reference Architecture featuring the PXIe-4468 Signal Generator with the Data Converter Validation Module software.

The Converter

The device under test (DUT) is the AD7606B, an eight-channel, 16-bit A/D converter from Analog Devices that supports sampling at throughput rates of 800 kS/s for all channels. The device input range is hardware selected and configured to ±5 V. The device is also configured to use the internal 2.5 V reference and hardware configured for a 16-bit parallel output. The parallel data output is controlled by RD and CS while the conversion is started with CONVST.

Hardware Setup

The Data Converter Validation Reference Architecture features the following NI hardware:

- PXIe-4468 Analog Source
- PXIe-40x1 Digital Multimeter
- PXIe-657x Digital Capture/DUT Control/Clock
- PXIe-109x Chassis
- PXIe-888x Controller

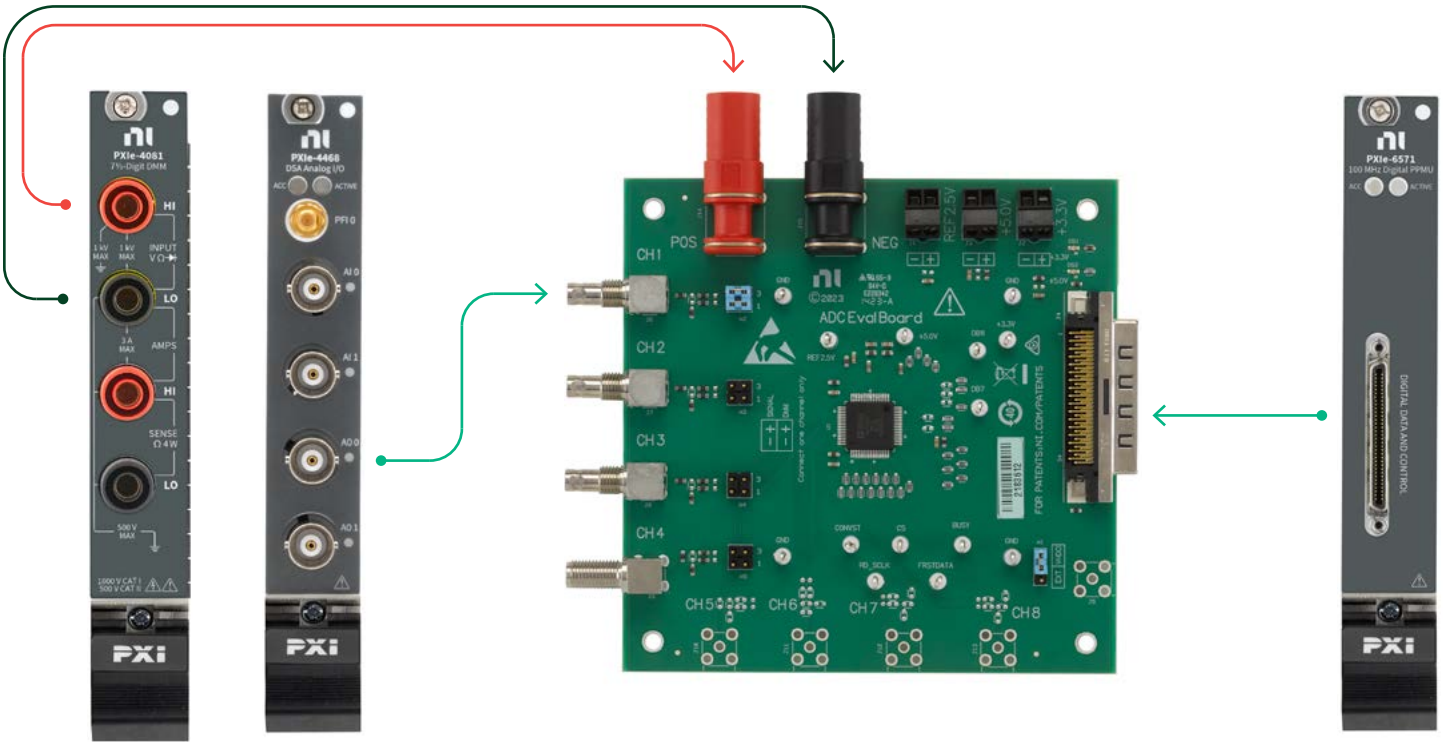

FIGURE 01

The test system uses the PXIe-4081 Digital Multimeter, the PXIe-6570 Digital Pattern Instrument, the PXIe-1095 chassis, and the PXIe-8840 Controller.

Evaluation Board

The AD7606B evaluation board was designed by NI to be used with the Data Converter Validation Module and makes connectivity to NI instrumentation easier.

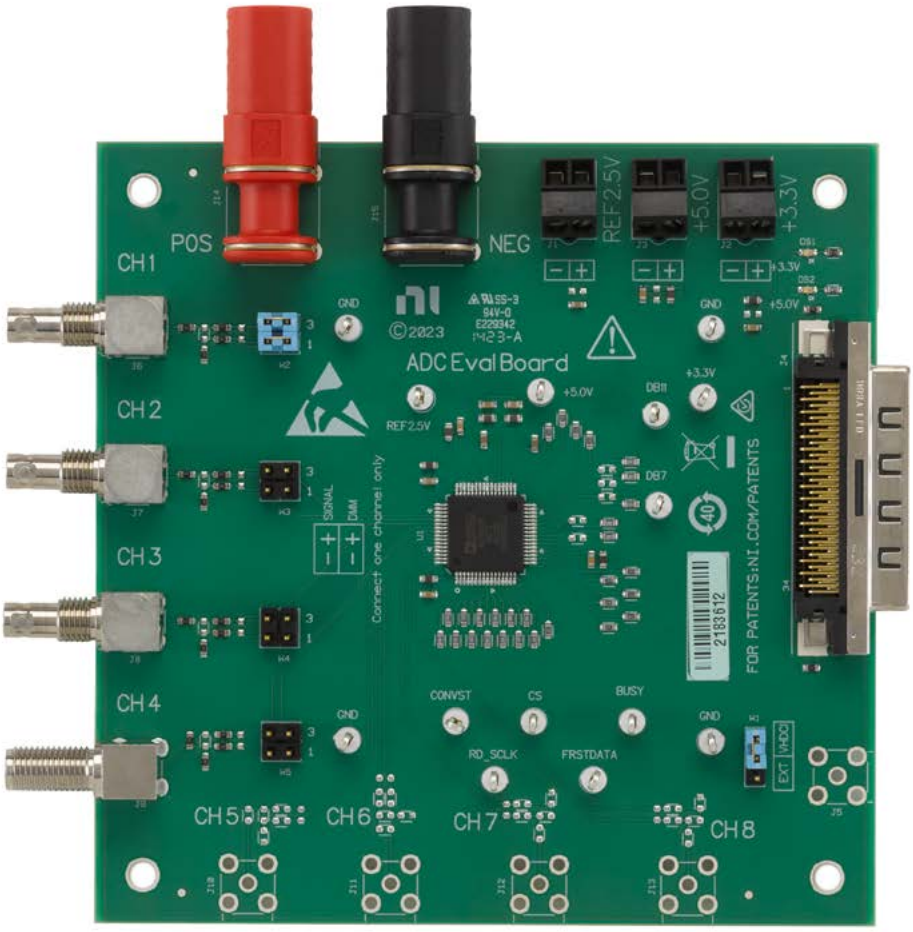

FIGURE 02

AD7606B Evaluation Board

Power

The evaluation board provides the +3.3 V and +5 V power supply to the DUT. The 2.5 V reference is optional.

Digital

The digital lines from the ADC are routed to the VHDCI connector on the right side of the board. This is meant to connect directly to a PXI-657x device with a VHDCI-VHDCI cable. The mapping of the signals to a PXI-657x are as follows:

View Connections for: All Pins and Relays

Pin	Site	Instrument	Channel
DB0	0	PXI2Slot7	0
DB1	0	PXI2Slot7	1
DB2	0	PXI2Slot7	2
DB3	0	PXI2Slot7	3
DB4	0	PXI2Slot7	4
DB5	0	PXI2Slot7	5
DB6	0	PXI2Slot7	6
DB7	0	PXI2Slot7	7
DB8	0	PXI2Slot7	8
DB9	0	PXI2Slot7	9
DB10	0	PXI2Slot7	10
DB11	0	PXI2Slot7	11
DB12	0	PXI2Slot7	12
DB13	0	PXI2Slot7	13
DB14	0	PXI2Slot7	14
DB15	0	PXI2Slot7	15
CONVST	0	PXI2Slot7	16
OS0	0	PXI2Slot7	17
OS1	0	PXI2Slot7	18
OS2	0	PXI2Slot7	19
SCLK	0	PXI2Slot7	20
CS	0	PXI2Slot7	21
BUSY	0	PXI2Slot7	22
FRSTDATA	0	PXI2Slot7	23
SDI	0	PXI2Slot7	24
DOUTA	0	PXI2Slot7	25
DOUTB	0	PXI2Slot7	26
DOUTC	0	PXI2Slot7	27
DOUTD	0	PXI2Slot7	28
RESET	0	PXI2Slot7	29

FIGURE 03

Mapping Signals to a PXI-657x

Analog Source Connectivity

The evaluation board includes connectors for the first four channels. Channels 1–3 are HD-BNC connectors and can interface to the dynamic signal generator PXIe-4468. Channel 4 is an SMA connector and can be connected to an arbitrary waveform generator such as the PXIe-54x3.

DMM Connectivity

For tests which rely on precision DC measurements such as gain and offset and code transitions (full-scale error), a DMM is required to provide the necessary DC accuracy for calculations. The banana plugs on the top of the board can be used to connect a DMM to one of the analog channels (1–4) input paths using jumpers.

Full-Scale Error

The full-scale error measurement calculates three code transitions and their deviation from the ideal position. The code transitions are:

Bipolar Zero Code: The midscale transition where codes change from all 1s to all 0s

Positive Full-Scale Code: The last code transition

Negative Full-Scale Code: The first code transition

The error is the difference between the measured code transition and the ideal code transition typically expressed in LSBs.

To find the actual code transition, the dynamic signal generator (PXIe-446x) will generate a DC voltage in a range and step size defined by the user. At each voltage step, a DMM (PXIe-40x1) measures the input voltage at the ADC and the ADC acquires multiple samples. Multiple samples are necessary to reduce the effect of the ADC's input referred noise on the code transition measurement. After the test has progressed through each DC voltage step, an algorithm interpolates where the actual code transition is located.

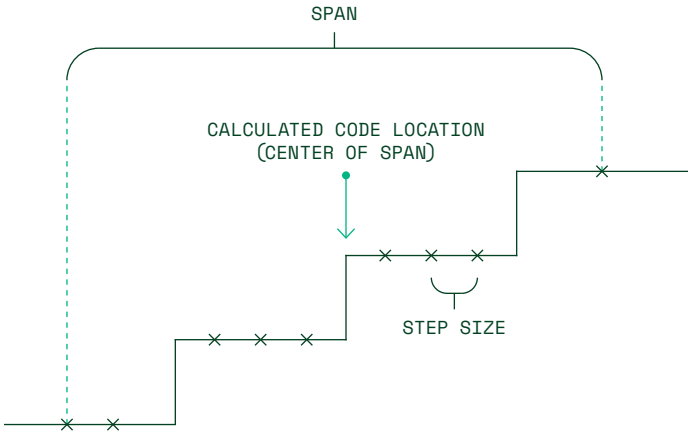

FIGURE 04

Finding Code Transition

Measurement Settings

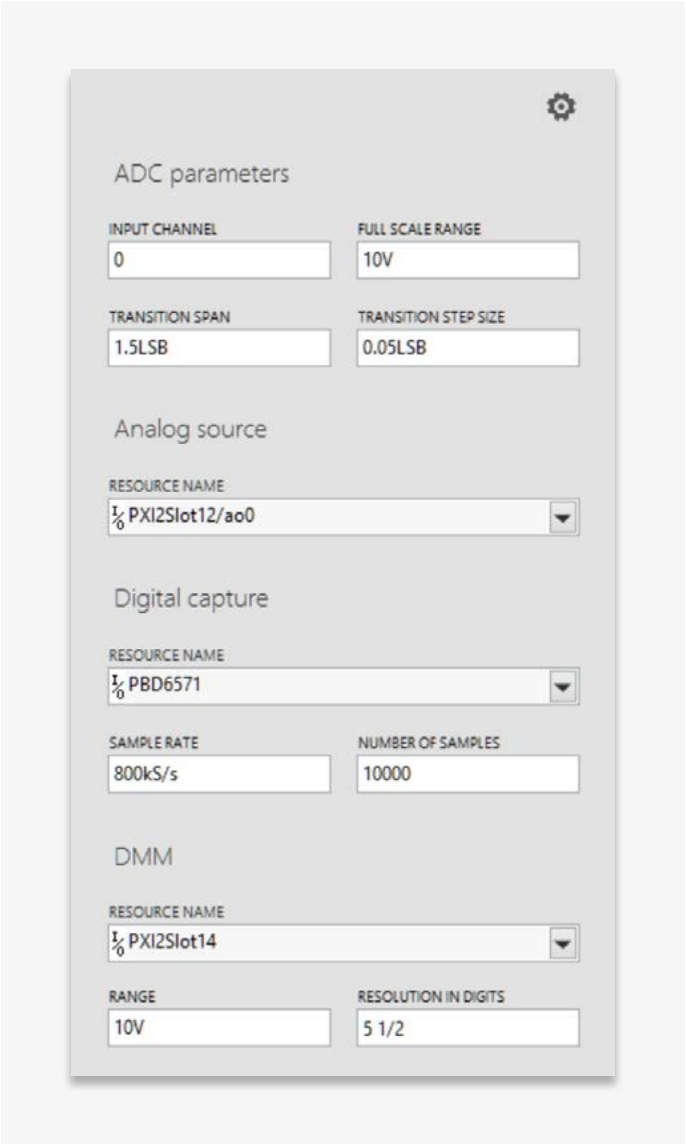

FIGURE 05

Measurement Settings

The measurement settings allow for customization of the full-scale error measurement. The ADC parameters should be configured to specify which channel of the DUT is being tested and the full-scale range setting of the device. The transition span and step size can be adjusted to impact test time and accuracy of the measurement. In a scenario where a transition was not captured by the measurement instrumentation (see Figure 6), increasing the span can improve the likelihood of seeing the transition.

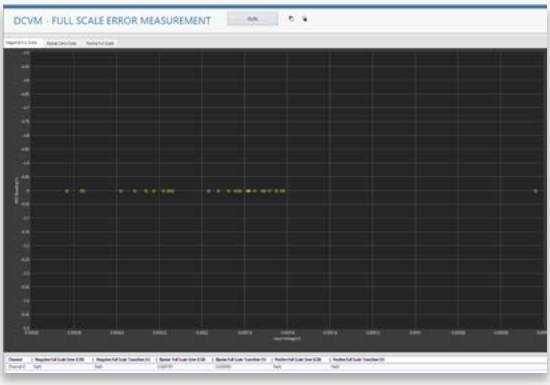

FIGURE 06

A DCVM full scale error measurement scenario where a transition was not captured by the measurement instrumentation.

For our specific test, channel 0 of our DUT is the test channel. The DUT has a sample rate of 800 kS/s and was hardware configured to have a 10 V full-scale range. The PXIe-4081 Digital Multimeter is a 7.5-digit DMM, but it was configured to 5.5 digits to improve test time.

FIGURE 07

A DCVM full scale error measurement scenario showing a subset of raw data for a negative full-scale error measurement.

Figure 7 shows a representative subset of the raw data for a negative full-scale error measurement in graph form. While the measurement was set up to collect 10,000 samples, each sample is not displayed. The transition from the first code can be approximated visually and the calculated data from the interpolation algorithm can be read from the table underneath the graph. The voltage of the transition as well as full-scale error in LSBs is calculated and displayed.

Linearity

In data converters, there are two measurements of the linearity of its transfer function: integral nonlinearity, relative accuracy (INL) and differential nonlinearity (DNL). In ADCs such as our DUT, INL is the deviation between the ideal input threshold value and the measured threshold level of a certain output code. DNL is the deviation between two analog values corresponding to adjacent input digital values. It is the difference between an actual step width and the ideal value of 1 LSB.

The Data Converter Validation Module uses the histogram test, or code density test, to determine nonlinearity parameters such as INL and DNL. This approach is performed in the amplitude-domain of a data converter. A repetitive and dynamic signal with a bathtub distribution, such as a sine-wave signal, is applied to the ADC, generating a corresponding distribution of digital codes at the output of the converter. Any deviation from the corresponding output code distribution results in various errors that may be estimated with the histogram method, including INL and DNL.

Measurement Settings

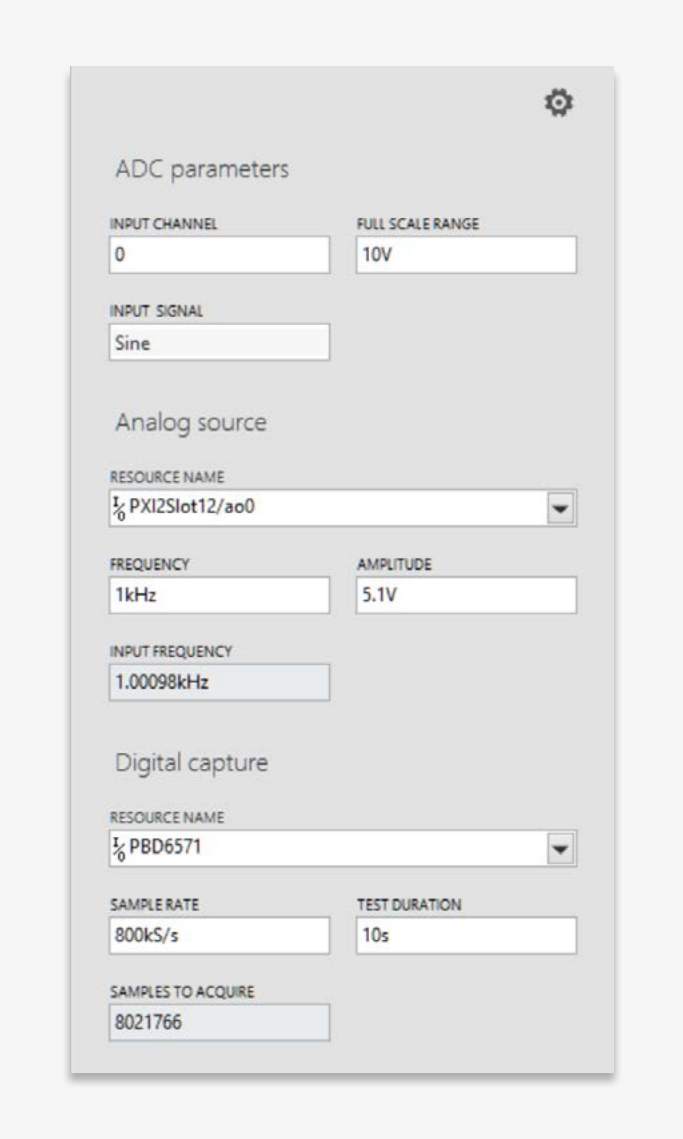

FIGURE 8

Measurement Settings

The measurement settings allow for customization of the linearity measurement. The ADC parameters should be configured to specify which channel of the DUT is being tested and the full-scale range setting of the device. The input signal can be configured to be a sine wave, a triangle wave, or a non-repeating ramp. Additionally, the frequency and amplitude of the analog source can be configured. To hit all the ADC codes, it is recommended to have the sine wave amplitude 10 percent greater than the input range of the ADC. The user can also configure the ADC sampling rate and the test duration. The sine wave frequency will be coerced to a value that is relatively prime to the sampling rate and defined in this equation from IEEE 1241:

$$f_i = \left(\frac{J}{M}\right) f_s$$

where

f is an integer which is relatively prime to M

f_s is the sampling frequency

M is the record lenght

The test duration will be coerced to the nearest values which allow for an integer number of sine wave cycles to be acquired. The signal generator outputs the sine wave, and the ADC acquires the time domain data. There is no hardware synchronization between the signal generator and the ADC. The histogram of the time domain data is computed and the difference between the measured and ideal histogram is used to calculate the differential and integral nonlinearity.

Histogram

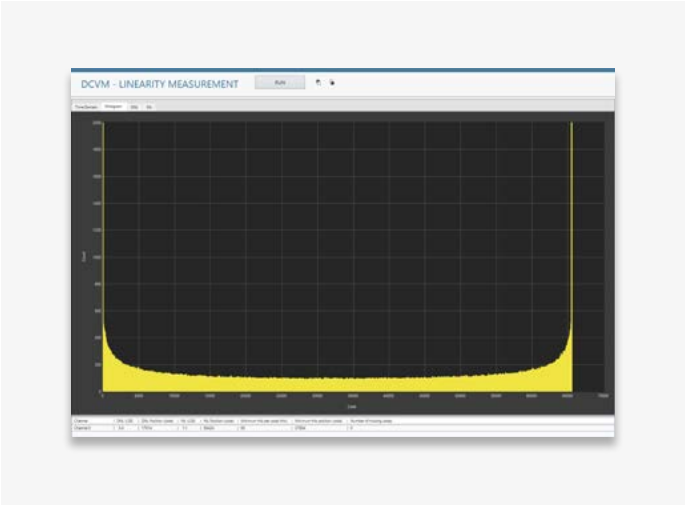

FIGURE 09

Histogram

DNL

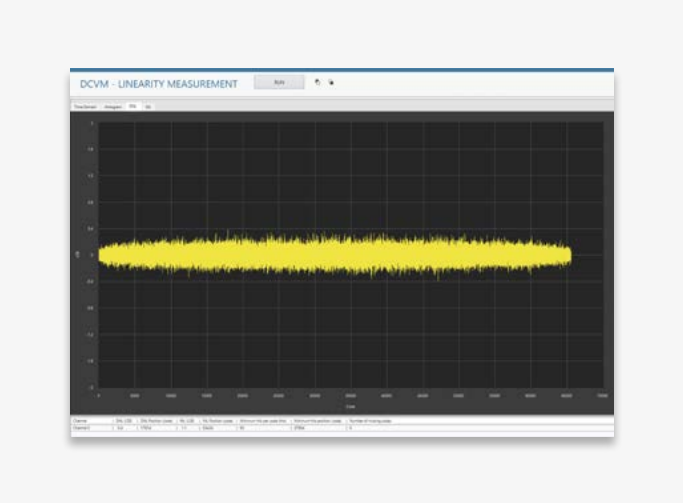

FIGURE 10
Differential Nonlinearity

INL

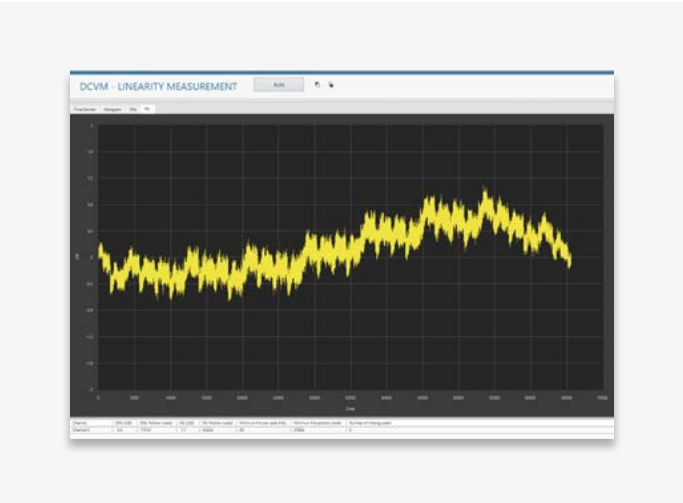

FIGURE 11
Integral Nonlinearity

AC Measurements

Included in AC measurements are SNR, SINAD, THD, SFDR, and ENOB. Signal-to-noise ratio (SNR) is a calculated value that represents the ratio of the RMS level of the input signal to RMS noise. Signal-to-noise and distortion ratio (SINAD) is similarly the ratio of the RMS level of the input signal to the RMS value of the root-sum-square of all noise and distortion components in the FFT analysis, excluding the DC components. In ADCs, spurious free dynamic range (SFDR) is the ratio of the RMS amplitude of the carrier frequency (maximum signal

component) to the RMS value of the next largest noise or harmonic distortion component. Effective number of bits (ENOB) is calculated from SINAD using the relationship for the theoretical SNR of an ideal N-bit ADC. The equation follows.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

In this equation, SINAD is the power ratio in dB, 6.02 is the divisor that converts decibels to bits, and 1.76 is the term that comes from the quantization error in an ideal ADC. Additionally, while total harmonic distortion plus noise (THD+N) is not an included measurement, its value is equivalent to the inverse of SINAD in that it is the sum of all spectral components of the test tone (excluding the test tone itself) over a certain bandwidth.

Measurement Settings

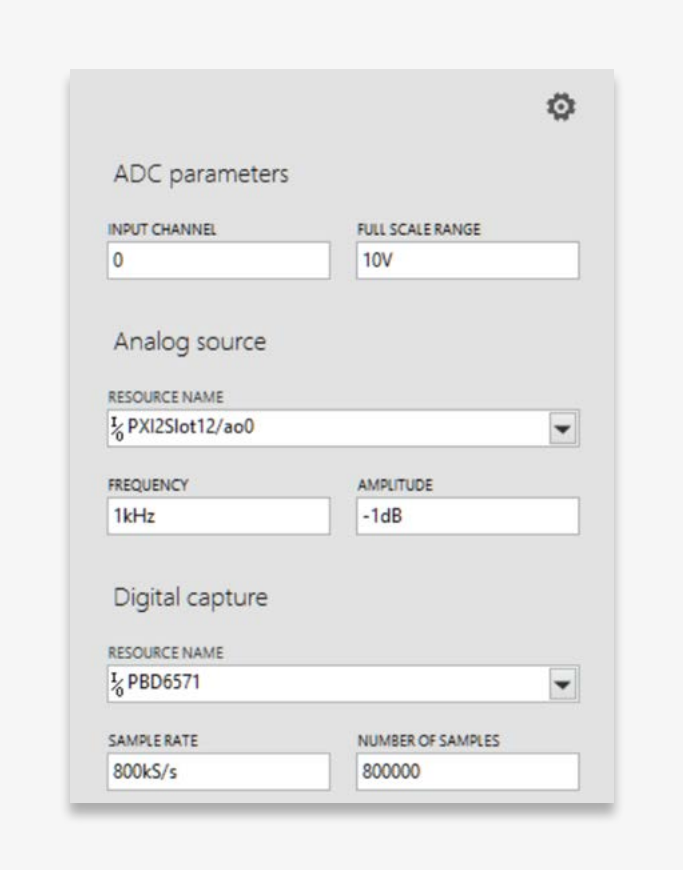

FIGURE 12

Measurement Settings

The measurement settings allow for customization of the AC measurements. The ADC parameters should be configured to specify which channel of the DUT is being tested and the full-scale range setting of the device. The signal generator outputs a sine wave of the user specified frequency and amplitude. The user also specifies the number of samples and the sampling rate of the ADC acquisition. There is no hardware synchronization between the signal generator and the ADC. A seven-term Blackman-Harris window is applied to the acquired time domain data from the ADC before the dynamic measurements such as THD and SFDR are calculated. This methodology is described in IEEE 1241 section 8.8.1.2.

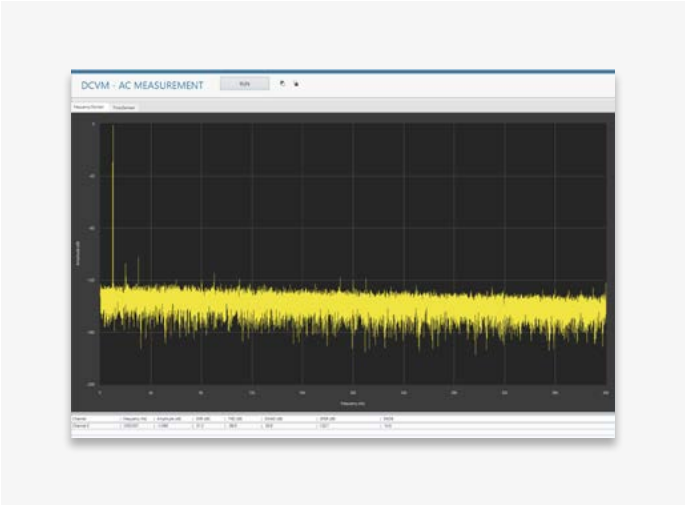

FIGURE 13

Customization of the AC Measurements

Gain and Offset

Offset error is defined as the deviation between the first actual code transition and the first ideal code transition, which should take place at 0.5 LSB. This offset error can be positive or negative and limits the available range of the ADC.

Gain error is defined as the deviation of the midpoint of the last step of the ideal ADC from the midpoint of the last step of the actual ADC, compensating for the offset error. It is a measurement of the deviation in slope of the actual ADC transfer characteristic from the ideal.

Measurement Settings

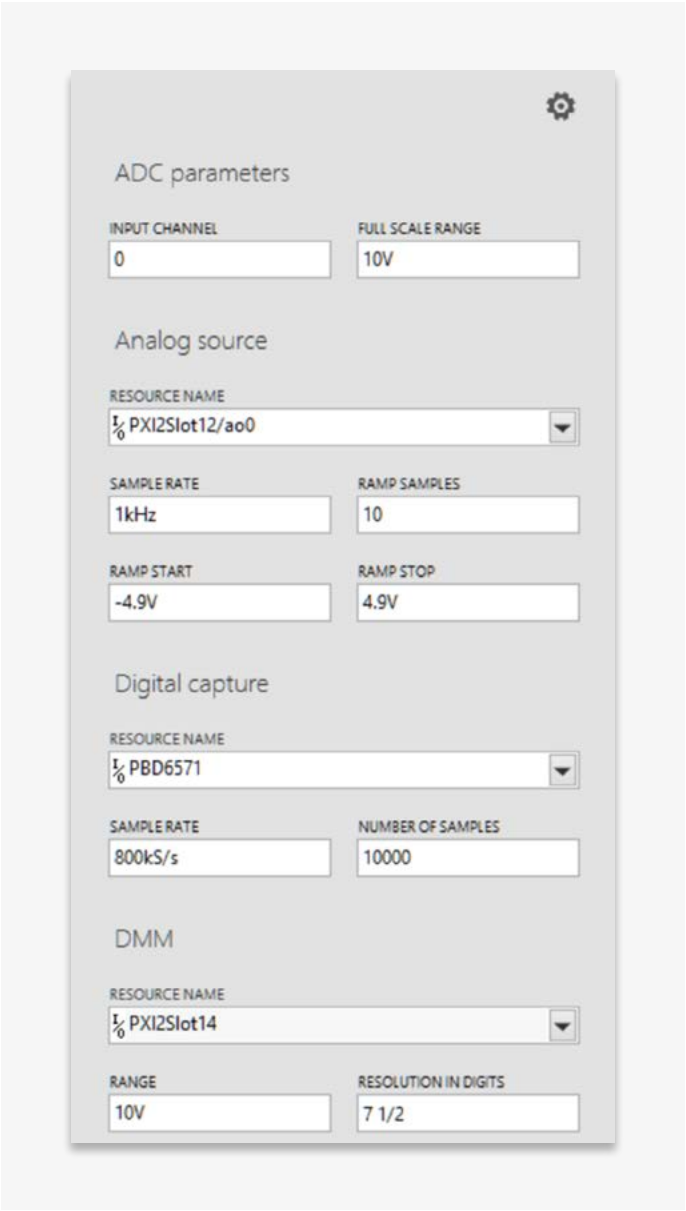

FIGURE 14

Measurement Settings

The user configures a voltage range and number of steps for the measurement. At each step, the signal generator outputs a DC voltage. The DC voltage is measured by both the DMM and ADC. The measured value for each is stored and the process repeats until the last voltage is reached. The gain and offset are determined by least squares fit using the DMM and ADC voltage measurements.

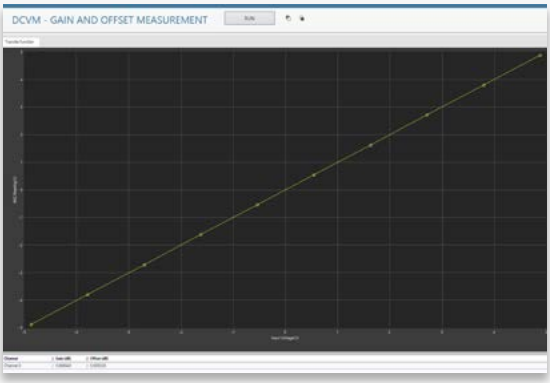

FIGURE 15

Data Converter Validation Module

NI's Advantage for Data Converter Testing

NI's solution for data converter testing includes multiple modules within a single PXI chassis. Leveraging the PXI platform allows NI to take a modular approach to automated test. Any PXI module can be added to a tester and programmed accordingly. This means users are not limited to a specific set of devices that may become obsolete and require the purchase of an entirely new tester. Likewise, as test needs and volume change over time, modules may be repurposed accordingly. Because the instrumentation resides within a single PXI chassis, these modules can communicate and synchronize seamlessly.

Of the more than 1,500 PXI products on the market, more than 600 were designed by NI. In particular, the PXIe-4468 Analog Source brings benchtop quality noise and distortion performance in PXI form factor. NI is continually pushing the boundaries of performance with its PXI modular instruments in a more efficient 3U space.

The Data Converter Validation Module provides a simple-to-use software solution that allows for a fast bring-up with ready-to-run measurements in InstrumentStudio™ software and TestStand™. In addition to facilitating a seamless transition from interactive bench top measurements to automated validation, the software also allows for interactive debug monitoring during automated testing.